AD-A036 691

MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

VOLUME IV. 1976 ANNUAL REFERENCE SUPPLEMENT

(DOCUMENT NUMBERS 11045-11745)

IIT RESEARCH INSTITUTE
CHICAGO

PREPARED FOR
ROME AIR DEVELOPMENT CENTER
GRIFFISS AIR FORCE BASE, NEW YORK

APRIL 1976

MRB 0474 Vol. IV

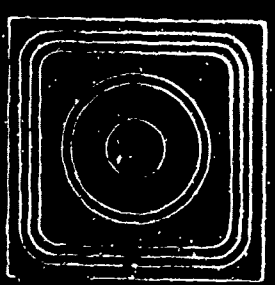
APRIL 1976

MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

Volume IV - 1976 ANNUAL REFERENCE SUPPLEMENT

(DOCUMENT NUMBERS - 11045 - 11745)

RAC



Reliability Analysis Center

ROME AIR DEVELOPMENT CENTER

THE RELIABILITY ANALYSIS CENTER IS A DOD INFORMATION ANALYSIS CENTER

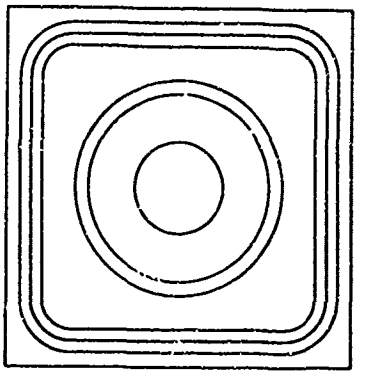
NOTICE:

The MICROCIRCUIT RELIABILITY BIBLIOGRAPHY is reissued annually each April. To keep current reference information on hand purchase of the updated issue is recommended after April 1977.

The Reliability Analysis Center is a DoD Information Analysis Center

operated by IIT Research Institute

under contract to the Rome Air Development Center, AFSC



The Reliability Analysis Center (RAC) is a service for the dissemination of reliability and experience information on microcircuit devices, including integrated circuits, thick and thin film circuits, hybrid devices, and large scale arrays (LSI) employed in military, space and commercial application.

The RAC analyzes and disseminates information that is generated during all phases of device fabrication, testing, equipment assembly, and operation. RAC data files are continually updated through information collected from independent R&D testing laboratories, device and equipment manufacturers, government agencies, and field installations.

REQUESTS FOR TECHNICAL ASSISTANCE AND INFORMATION ON AVAILABLE RAC SERVICES AND PUBLICATIONS MAY BE DIRECTED TO

Harold A. Lauffenburger
Reliability Analysis Center (RBRAC)
Rome Air Development Center
Griffiss Air Force Base, NY 13441
Telephone: 315/330-4151
Autovon: 587-4151

ALL OTHER REQUESTS SHOULD BE DIRECTED TO

Rome Air Development Center
RBRD/Anthony J. Feduccia
Griffiss Air Force Base, NY 13441
Telephone: 315/330-4921
Autovon: 587-4921

RELIABILITY ANALYSIS CENTER

A DOD INFORMATION ANALYSIS CENTER

MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

MRB 0474 Vol. IV

1976 Annual

Reference Supplement

Date of Issue: April 1976

Prepared By:

IIT RESEARCH INSTITUTE
10 WEST 35 STREET
CHICAGO, ILLINOIS 60616

Under Contract To:

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

INTRODUCTION

GENERAL

The Microcircuit Reliability Bibliography references literature pertinent to the reliability of microcircuit technology. Aspects found herein encompass design, fabrication, quality assurance and application. References are selected for citation from the Reliability Analysis Center document files. The portion of the collection presented here dates from acquisitions made during 1967 (the inception of the RAC) to March of this year. Documents are selected on the basis of informational currency and usefulness, as well as availability to the engineering community. Unpublished data and related matter not generally disseminated by the primary source or through government agencies (e.g. DDC or NTIS) or industry channels are excluded.

FORMAT

Volumes IB, II, III and IV comprise an updated index and complete set of abstract citations.

MRB Volume I-B: Cumulative Index, April 1976
MRB Volume II: Cumulative References, April 1974
MRB Volume III: 1975 Annual Reference Supplement, April 1975
MRB Volume IV: 1976 Annual Reference Supplement, April 1976

The reader may discard volume IA, MRB Index 1975, without loss since this information is now obtained in Volume IB.

Volume IB: the Cumulative Index, is an index to material found in both volumes II, III and IV Volume IB is prepared in photo-ready format by computerized techniques.

Volume II: MRB Cumulative References provides complete coverage of RAC bibliographic citations through February 1974.

Volume III: MRB 1975 Annual Reference Supplement provides additional bibliographic coverage through March 1975.

Volume IV: MRB 1976 Annual Reference Supplement provides additional bibliographic coverage for the current year.

CONTENT

Volume IB Cumulative Index

The index contains the following four sections:

Term Selection Guide
Subject Term Index
Corporate Author Index
Personal Author Index 1976

Section I — **TERM SELECTION GUIDE:** contains subject terms selected from the RAC microcircuit Thesaurus. The terms are arranged in alphabetical order with sub-term description following each main term. For the reader's convenience, extensive cross-referencing is provided. The Selection Guide has been expanded this year to reflect some of the recent changes in technology.

Section II — **SUBJECT TERM INDEX:** Cross-references subject terms and the RAC assigned document identification numbers found in Volumes II and III. In addition, all documents are assigned by computer, to one or more of the following reliability related categories.

1. Failure Analysis: Evaluation of defects, and failure analysis techniques.
2. Test Procedures: Reliability Test techniques and procedures, including process control techniques.
3. Fabrication Method and Techniques: Reliability aspects of microcircuit manufacturing.
4. Reliability Studies: Technical reports relating to formal reliability studies and investigations.
5. Computer Analysis: Math Modeling & Prediction: Prediction and modeling, statistical tools, Weibull analysis computer analysis, computer aids, etc.
6. Miscellaneous: Cites references that were not designated in any of the above categories.

Section III — **CORPORATE AUTHOR INDEX:** An alphabetical listing of selected corporate authors (i.e. names of organizations) originating documents. Each corporate author is followed by a listing of the appropriate RAC document identification numbers.

Section IV — **PERSONAL AUTHOR INDEX 1976:** An alphabetical listing of personal authors found in the Annual Reference Supplement with corresponding citation title and RAC document identification number.

Volumes II, III and IV — **CUMULATIVE AND ANNUAL REFERENCES**

Volume II, MRB Cumulative References provides complete coverage of RAC bibliographic citations from 1967 through February 1974. References cited in Volume II are ordered sequentially with RAC assigned document identification numbers 1401 through 10414. Each citation includes (wherever possible) document title, author, source organization, identifying designations, in addition to a fully descriptive abstract of its content.

Volume III, MRB 1975 Annual Reference Supplement provides the additional bibliograhic coverage from March 1974 to March 1975. RAC-assigned document numbers for this publication are 10417 through 11044. The citation format is the same as in Volume II.

Volume IV, MRB 1976 Annual Reference Supplement provides additional bibliographic coverage from March 1975 through March 1976. RAC-assigned document numbers for this volume are 11045 through 11745. Citation format is the same as used in Vols. II & III.

Gaps in the numbering sequence are due to selection. Because hard-to-acquire documents are not included, the cited references for certain subjects are necessarily incomplete. Thus, the RAC files may contain substantially more information or data than indicated in the bibliography. Complete data and guidance information are available from RAC published data compendia or direct consultation with RAC staff personnel.

Section V **DOCUMENT TITLE - KEYWORD IN CONTEXT INDEX 1976:** An alpha-numerical listing of keywords from the document title which provides multiple means for uncovering document accession numbers.

ORDERING INFORMATION

The reader may order additional copies of the MRB or previously issued volumes directly from the Reliability Analysis Center. Pricing information follows:

Current issues		
(Vol. IB and Vol. IV)	**$ 40.**	($80. foreign)
Complete four volume set		
(Vols. IB, II, III and IV)	**$ 50.**	($100. foreign)

HOW TO OBTAIN DOCUMENTS REFERENCED IN THIS BIBLIOGRAPHY

Each reference listed herein contains complete bibliographic information including the personal and corporate author with address. Where the document is available from one of the government document distribution centers listed below, the cited reference will include an order number (e.g. AD, N, DP, etc.). Other documents can be obtained from the original source (i.e. author, journal, society, etc.). **DOCUMENTS OTHER THAN THOSE PUBLISHED BY RAC CAN NOT BE OBTAINED FROM RAC.**

To determine the availability of AD documents write or phone:

National Technical Information Service
(NTIS)
5285 Port Royal Road
Springfield, Virginia 22161
(703) 557-4650

OR for AD or AD Limited documents if you are a government contractor, contact:

Defense Documentation Center
(DDC)
Cameron Station
Alexandria, Virginia 22314
(202) 274-7633
Autovon: 284-7633

OR to determine the availability of N documents

NASA Scientific and Technical Information Facility
Post Office Box 8757
Baltimore/Washington International Airport
Maryland 21240
(301) 796-5300

HOW TO USE THE BIBLIOGRAPHY

PROCEDURE

1) Select a bibliographic term(s) from the **Term Selection Guide (Section I)** that most closely agrees with your subject interest.

2) Look up the selected term(s) in the categorized **Subject Term Index (Section II)** to obtain a list of document numbers.

   a) The terms of interest may be found under one or more categories. By choosing a category pertinent to your subject interest, a two-term logical AND is automatically achieved.

   b) Additional terms may also be utilized in combination for AND/OR logical searches. For an AND situation a document number must appear under EACH of the terms searched in order for it to satisfy the search criteria. For an OR situation, all document numbers appearing under any one of the terms searched satisfy the criteria. The terms may all be in a single category or the search may encompass several categories.

3) If interested in reports issued by a specific organization, locate them in the **Corporate Author Index (Section III)** and read corresponding document numbers. Corporate Author may be combined with subject terms for an AND or OR type search statement.

4) If interested in reports by a specific author issued after March 1, 1974 locate them in the **Personal Author Index (Section IV)** and read the corresponding titles and document numbers.

5) If searching for documents by title, consult the **Document Title - Keyword in Context Index (Section IV)** for the appropriate accession numbers. (This Index covers 1976 accessions only).

6) After pertinent document numbers are identified, go to Volume II, III or IV to obtain the bibliographic and abstract information.

EXAMPLE SEARCH

Problem: Suppose you are interested in locating references to help in the evaluation of your screening program.

Solution:

1) Scan the **Term Selection Guide (Section I)** for subject terms related to your problem. For this example you could choose the term SCREENING EFFECTIVENESS. Turning to the **Subject Term Index (Section II)**, you may decide that Category 2: Test Procedures is the subject you wish to reference. In the Test Procedures chapter of Section II you will find the following document numbers listed under SCREENING EFFECTIVENESS:

1741	4825	10063	10162	10370	10738	11081	11615
3040	4829	10095	10247	10462	10976	11207	11620
4757	10014	10110	10251	10642	10980	11290	
4759	10052	10113	10254	10647	10989	11433	
4799	10060	10151	10258	10699	11032	11443	

2) The bibliographic information and abstracts for the document numbers less than 10415 are found in Volume II. The remaining document numbers are found in Volume III and IV.

3) If you wish to qualify the search to a specific technology, such as complementary, MOS (CMOS), follow the same procedure as above.

a) Locate the term CMOS in the **Term Selection Guide (Section I)**

b) Referring to the **Subject Term Index (Section II)** under Category 2 Test Procedures, you will find the following document numbers listed under the term CMOS:

3071	4769	10218	10775	11191	11497	11704
4093	10018	10260	10954	11207	11689	11710
4435	10063	10262	10989	11258	11691	
4760	10081	10738	11044	11394	11694	

c) Comparing the two document lists for coincident document numbers yields the following results for test procedures related to screening effectiveness for CMOS devices.

10063 10738 10989 11207

(Document numbers 10063, 10738 and 10989 are found in Volume II, while 11207 appears in Volume IV)

ADDITIONAL INFORMATION

The documents referenced may be acquired from the originator, the publisher, or one of the government document dissemination agencies. Ordering details appear under **HOW TO OBTAIN DOCUMENTS REFERENCED IN THIS BIBLIOGRAPHY.**

Please contact the RAC directly for further information concerning indepth literature searches, published reliability data compendia and technical consulting assistance.

11045

Fox, W.A. (Natl. Semiconductor Corp., Santa Clara, CA)
A 16-BIT MICROPRCCESSOR. pp. 16-7. 1975 IEEE International Solid-State Circuits Conference

The architecture of the PACE (Processing and Control Element) microprocessor has been organized to minimize external components, yet to provide a powerful instruction set for data manipulation and input/output. It is a parallel 16-bit, single-chip CPU implemented in P-channel, silicon-gate technology. PACE features four general purpose accumulators, a 10-word stack, interrupt logic control and status flags, a 16-bit ALU, and requires single phase, true and complement clocks. It has forty-five instruction types (337 individual instructions) with a typical execution time of 10 microseconds.

11046

Wen, D.D., Early, J.M., Kim, C.K. et al. (Fairchild Semiconductor, Palo Alto, CA)
A DISTRIBUTED FLOATING-GATE AMPLIFIER IN CHARGE-COUPLED DEVICES. pp. 24-5. 1975 IEEE International Solid-State Circuits Conference

A report on the operation of a distributed floating-gate amplifier which employs twelve charge-amplifying stages to sense extremely small charge packets in a buried channel charge-coupled device. Signal charges ranging from 30 to 10^5 electrons have been detected with an estimated rms noise equivalent signal of approximately 10 to 20 electrons at room temperature and 3-MHz bandwidth.

11047

Koike, N., Ashikawa, M., Kamiyama, T. et al. (Hitachi Central Res. Lab., Tokyo, Japan) AN ULTRA HIGH-SPEED CLOCK-PULSELESS SCANNER FOR MOS IMAGE SENSORS. pp. 26-7. 1975 IEEE International Solid-State Circuits Conference

A clock-pulseless scanner for MOS image sensors is described in this paper. The scanner can be highly instrumental in solving two major technical problems which have been believed to be inevitable in MOS sensors: slow scan rate, and low S/N ratio due to the spike noise.

11048

Jespers, P. and Millet, J.M. (Catholic U. of Louvain, Louvain-la-Neuve, Belg.)
A THREE-TERMINAL CHARGE-INJECTION DEVICE. pp. 28-9. 1975 IEEE International Solid-State Circuits Conference

This article discusses the development, fabrication, and electrical characteristics of a three terminal charge injection device.

11049

Brown, D.M., Ghezzo, M. and Garfinkel, M. (GE Corporate Res. and Dev. Schenectady, NY)
TRANSPARENT METAL OXIDE ELECTRODE CID IMAGER ARRAY. pp. 34-5. 1975 IEEE International Solid-State Circuits Conference

The use of metal oxide transparent electrodes in a high density charge injection imager device (CID) array has increased the sensitivity and has flattened and extended the spectral response to shorter wavelengths in the blue (4000A). Experimentally determined spectral-response curves of operational self-scanning CID imager arrays are presented.

11050

Craven, R.B. (Analog Devices/Semiconductor, Wilmington, MA)
AN INTEGRATED CIRCUIT 12-BIT D/A CONVERTER. pp. 40-1. 1975 IEEE International Solid-State Circuits Conference

A number of monolithic digital-to-analog converter circuits which use precision resistor ladder networks to determine the bit weighting have been developed. Efforts to extend these techniques to 12 bits have been inhibited both by the poorer yield of the resulting larger chips, and by the inability to deposit sufficiently precise resistors to realize 12-bit accuracy. This paper will describe an integrated circuit 12-bit D/A converter which circumvents these problems by combining bipolar LSI, Si-Cr on silicon, and active laser trimming technologies.

11051

Hamade, A.R. and Albarran, J.F. (Natl. Semiconductor Corp., Santa Clara, CA)
A JFET/BIPOLAR 8-CHANNEL ANALOG MULTIPLEXER. pp. 42-3. 1975 IEEE International Solid-State Circuits Conference

The recent trends towards digital implementation of analog control functions has made the need for a low cost, high performance analog multiplexer that uses JFET switches and bipolar drive circuitry. It has been fabricated on a 4700 mil^2 monolithic silicon chip using a new JFET/bipolar process. Each of the eight switches exhibits a typical 'on resistance' of 200 which is not modulated by the analog range of $\pm$ 10 V in less than 1 s. The circuit uses a bias scheme which assures operation over a wide range of temperature and process variations.

11052

Hornak, T. and Corcoran, J. (Hewlett-Packard Labs., Palo Alto, CA)
A HIGH PRECISION COMPONENT-TOLERANT ADC. pp. 44-5. 1975 IEEE International Solid-Sate Circuits Conference

Converters based on two resistors or two capacitors have been described. More typically, a ladder of many resistors is used. In the converter to be described, precision is based on the ratio accuracy of a small pulse transformer with tightly coupled windings. This ratio accuracy is known to be highly predictable and essentially independent of temperature and time. AC calibration systems and ac D/A converters have used the ratio precision of transformers for years. The conversion technique discussed allows the transformer to be used to encode dc signals.

11053

Dill, F.H. (IBM, T.J. Watson Res. Ctr., Yorktown Heights, NY)
POSITIVE OPTICAL LITHOGRAPHY. pp. 54-5. 1975 IEEE International Solid-State Circuits Conference

Optical lithography is the central pattern-determining technology in microelectronics. In this paper new techniques for quantitative understanding of lithography as applied to positive photoresist will be presented. These techniques involve a mathematical model based on physically measurable parameters; this enables computation of the effects of exposure and development on a photoresist film.

11054

Kriegler, R.J. (Bell-Northern Res., Ltd., Ottawa, Can.)
HIGH QUALITY SiO_2 FOR INTEGRATED CIRCUITS. pp. 56-7. 1975 IEEE International Solid State Circuits Conference

This paper will deal with four benefits that may be obtained from the use of HCl during high temperature processing of SiO_2: a reduction of instabilities due to the presence of mobile ions in the oxide, an improvement in the dielectric breakdown characteristics of the oxide, a reduction of the surface state density at the oxide-silicon interface, and an increase in the minority carrier life time in the underlying silicon.

11055

Le Carpentier, J. (RTC-La Radiotechnique-Compelec, Caen, Fr.)
COMPUTER AIDED SYNTHESIS OF AN IC ELECTRICAL DIAGRAM FROM MASK DATA. pp. 84-5. 1975 IEEE International Solid-State Circuits Conference

Computer-aided mask making is essential in integrated circuit development, but automation of layout design is not yet widely used. The designer must thus define his topology by hand or with the aid of a graphical display and errors may occur, which means that the layout is not in accordance with the electrical design. Full checking by hand being almost impossible, the remaining errors can only be detected after processing the slices when the costs and time spent are already high. Reliability is greatly improved if one can use a computer to check the correspondence between the layout coded for mask making and the electrical diagram. This is the aim of the VETO program (Verification of Topology).

11056

Foss, R. and Harland, R. (Microsystems Internatl., Ltd., Ottawa, Can.)
SIMPLIFIED PERIPHERAL CIRCUITS FOR A MARGINALLY TESTABLE 4k RAM. pp. 102-3. 1975 IEEE International Solid-State Circuits Conference

One-transistor-cell MOS RAMS have made feasible memory circuits with cell areas around 1 sq. mil. The problems associated with such circuits are well known. The signals used are small expressed in terms of charge, and the ratio of cell capacitance to bit-line capacitance is often 1:10 or more, dividing the storage node voltages by a corresponding ratio. Practical forms of such memories frequently use circuits peripheral to the array of such complexity as to negate much of the chip area advantage given by the one transistor cell. These circuits largely determine performance and power consumption as well as the susceptibility of the memory to pattern-sensitivity.

11057

Ebel, M., Gionis, J. and Regitz, W. (Intel Corp., Santa Clara, CA)
A 4096-BIT HIGH SPEED ECL COMPATIBLE RAM. pp. 104-5, 219. 1975 IEEE International Solid-State Circuits Conference

There is a well-defined area of the memory market involving high-speed ECL oriented systems for which fast access times with static operation are essential requirements. A unique dynamic MOS memory with a pseudostatic cell that meets these requirements will be described. The fully decoded memory is 4096 words of 1 bit and all inputs (including clocks) and outputs are fully ECL compatible. It is fabricated using the N-channel silicon-gate process on a monolithic 204 x 237 mil silicon chip and is assembled in a 22-pin dual-in-line package.

11058

Scharbert, J. and Murrmann, H. (Siemens AG, Munich, West Ger.)
A 1024-BIT ECL-PROM WITH 15 ns ACCESS. pp. 106-7. 1975 IEEE International Solid-State Circuits Conference

TTL-PROM devices with up to 2-kbit capacity and about 50-ns access have become industry standard. The aim or our investigation was to develop an ECL-PROM of 1-kbit capacity (256 words by 4 bit, ECL 10 k compatible) for high speed application with an address access of less than 25 ns.

11059

Uchida, Y., Endo, N., Saito, S. et al. (Toshiba Res. and Dev. Ctr, Kanagawa, Japan)
A 1024-BIT MNOS RAM USING AVALANCHE-TUNNEL INJECTION. pp. 108-9. 1975 IEEE International Solid-State Circuits Conference

This paper describes a 1024-bit nonvolatile MNOS random access memory using avalanche-tunnel injection and direct tunnel ejection for writing "0" and "1" respectively. Features of this memory are: no kind of isolation is required between memory cell array and peripheral circuits; writing both "0" and "1" can be done with single polarity power supply; unit cell size is comparable with that of the conventional MOS static RAM; and novel principle for writing operation and new memory cell array configuration have made it possible to implement this nonvolatile RAM.

11060

Swanson, R.M. and Meindl, J.D. (Stanford U., Stanford, CA)
FUNDAMENTAL PERFORMANCE LIMITS OF MOS INTEGRATED CIRCUITS. pp. 110-1. 1975 IEEE International Solid-State Circuits Conference

A reasonably simple technique for including both two dimensional and weak inversion effects in a short channel MOST model will be presented. This model is shown to impose a lower bound on obtainable propagation delay and power consumption for MOS circuits.

11061

Heller, L.G., Spampinato, D.P. and Yao, Y.L. (IBM, T.J. Watson Res. Ctr. Yorktown Heights, NY)
HIGH-SENSITIVITY CHARGE-TRANSFER SENSE AMPLIFIER. pp. 112-3. 1975 IEEE International Solid-State Circuits Conference

The one device dynamic memory cell, consisting of a single gating transistor and a storage capacitor, is attractive because of its low power consumption, its simple cell structure and its potential for high density. Density, however, is tied directly to the sensitivity of the detection circuit. It is the object of this paper to present a sense amplifier circuit with much better sensitivity than the standard latch circuit[1], while maintaining the feature of conveniently restoring the information in the cell.

11062

Graul, J., Kaiser, H., Kokkotakis, N.A. et al. (Siemens AG, Munich, West Ger.) and Ryssel, H. and Kranz, H. (Institut für Festkörpertechnolgie der Fraunhofergesellschaft, Munich, West Ger.)
DOUBLE IMPLANTED BIPOLAR HIGH-SPEED GATES WITH LOW-POWER DISSIPATION. pp. 120-1. 1975 IEEE International Solid-State Circuits Conference

This paper will report on a study of the speed power relations of oxide-isolated subnanosecond logic gates in relation to the characteristic data of double-implanted transistors (base-boron; emitter-arsenic). For comparison, double-diffused transistors (emitter-phosphorus) and circuits with conventional PN-isolation have also beeen assessed. Calculations of gate propagation delay versus power dissipation were performed with a modified Ebers-Moll model using measured transistor data and optimized geometrics.

11063

Rodgers, T.J., Asai, S., Pocha, M.D. et al. (Stanford U., Stanford, CA)
DMOS EXPERIMENTAL AND THEORETICAL STUDY pp. 122-3, 223, NSF ENG 74-12151. DAAB07-72-0229. 1975 IEEE International Solid-State Circuits Conference

Double-diffused MOS transistors (DMOST) have received attention as gigahertz discrete transistors, nanosecond high-density logic elements and 200-300V low resistance switches. DMOS transistors have short channel lengths achieved by the use of a double diffusion technique similar to bipolar processing. This paper will present two accurate two-transistor models for DMOS. The simple enhancement-depletion model (E/D) is an extension of previous efforts which includes velocity saturation effects. The full E/D model gives improved accuracy and is designed to predict DMOS characteristics in CAD programs by a two-device simulation.

11064

Ohta, K., Morimoto, M., Saitoh, M. et al. (Nippon Elec. Co., Ltd., Electrotech. Lab., Tokyo, Japan)
A HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED DEPLETION MOST. pp. 124-5, 224. 1975 IEEE International Solid-State Circuits Conference

This paper reports the results of an approach using Diffusion Self-Aligned Enhancement Depletion MOS ICs (DSA-ED-MOS IC). The results show the ns-pJ range performance of a high-speed logic LSI using DSA-ED-MOS IC together with the performance by other devices.

11065

Weckler, G.P. (Reticon Corp., Sunnyvale, CA)
THE SERIAL ANALOG PROCESSOR. pp. 142-3, 226. 1975 IEEE International Solid-State Circuits Conference

A general-purpose analog signal processing device with computational power exceeding conventional components will be described. Its principal function is that of a cross-correlator; however, it will also function as an analog memory. This device does not use charge transfer techniques. An alternate approach which offers distinct advantages for many applications has been developed.

11066

Copeland, M.A. and Roy, D. (Carleton U., Ottawa, Can.) and Chan, C.C. (Bell Northern Res., Ltd., Ottawa. Can.)
A MULTIPLEXED VIDEO BANDWIDTH CCD RELAY LINE. pp. 146-7. 1975 IEEE International Solid-State Circuits Conference

A multiplexed CCD analog delay line, capable of delaying a line of TV signals for applications such as synchronization and bandwidth compression, is described.

11067

Mattern, J. and Lampe, D. (Westinghouse Defense and Electronic Systems Center, Baltimore, MD)
A REPROGRAMMABLE FILTER BANK USING CCD DISCRETE ANALOG SIGNAL PROCESSING. pp. 148-9, 226. 1975 IEEE International Solid-State Circuits Conference

The Analog Shift Register (ASR) based on the charge-coupling principle may be used to implement a filter bank in the frequency band occupied by most doppler frequencies. In this application of the ASR, the time delays are controlled with digital precision while the analog processing is accomplished with operational amplifer accuracy. The number of independent filter characteristics equals the number of ASR stages available for data storage. Reprogramming of the filter is accomplished by replacement of three integrated memory circuits which control three sets of digital filter constants.

11068

Shott, J. and Melen, R. (Stanford Electronics Lab., Stanford, CA)
THE RAZORBACK CCD: A HIGH-PERFORMANCE PARALLEL INPUT DELAY LINE ARCHITECTURE. pp. 150-1, 227. N00014-67-A-0112-0044. 1975 IEEE International Solid-State Circuits Conference

There are many applications for analog signal delay lines. A CCD delay line with multiple input taps provides a versatile structure to satisfy many delay line requirements in a single device. The input taps of a multiple input CCD may be used: (1) singly to provide a selectable bit delay, or (2) in parallel to perform delay-sum and multiplexing signal processing operations.

11069

Sealer, D.A. and Tompsett, M.F. (Bell Labs., Murray Hill, NJ)
A DUAL-DIFFERENTIAL ANALOG CHARGE-COUPLED DEVICE FOR TIME-SHARED RECURSIVE FILTERS. pp. 152-3. 1975 IEEE International Solid-State Circuits Conference

Among the earliest proposed applications of charge-transfer devices was a digitally-controlled analog recursive filter in monolithic form. Subsequently, a second-order recursive filter using a bucket brigade device was reported.

11070

Anacker, W. (IBM, T.J. Watson Res. Ctr., Yorktown Heights, NY)
SUPERCONDUCTING TUNNEL DEVICES AS AN ALTERNATIVE TO SEMICONDUCTORS FOR FAST COMPUTER CIRCUITS. pp. 162-3. 1975 IEEE International Solid-State Circuits Conference

Analysis and experiments have demonstrated, the potential of superconducting Josephson tunneling circuits for very high performance computer circuits. Still, a host of problems exist, some of them unique to the new technology, but perhaps more of them due to the advancement toward higher system performance.

11071

Baechtold, W. (IBM Res. Lab., Zurich, Switz.)
A FLIP-FLOP AND LOGIC GATE WITH JOSEPHSON JUNCTIONS. pp. 164-5. 1975 IEEE International Solid-State Circuits Conference

The Josephson junction, a superconductive tunnel junction, shows great potential for very fast logic circuits due to its high switching speed and low power consumption. The first application of the device in a latching circuit was presented last year. In this paper, a new circuit, which is non-latching and, therefore, does not need a switched power supply, will be presented.

11072

Peltier, A.W. (Motorola Semiprod. Div., Mesa, AZ)
A NEW APPROACH TO BIPOLAR LSI: C^3L. pp. 168-9. 1975 IEEE International Solid-State Circuits Conference

Complimentary constant current logic (C^3L) is a dense, fast, efficient and producible form of bipolar LSI. Density is obtained from the simple NAND structure of the basic cell, which requires but one transistor regardless of the quantity of inputs or outputs. Gate array cells having five connectable outputs occupy ten to thirteen square mils of area for either triple diffused, V Isolation Polybackfill (VIP) or total dielectrically isolated realizations. Nearly 1,000 gating operations can be performed on a 130 mils square die. Switching speeds of 3 ns at 1.0 mW per gate to 100 ns at 0.01 mW per gate are attainable on the same die. At the cost of a complex metal system, the number and area of critical diffusions and the material sensitivity are reduced.

11073

Berger, H.H. and Wiedmann, S.K. (IBM Labs., Boeblingen, West Ger.)
SCHOTTKY TRANSISTOR LOGIC. pp. 172-3. 1975 IEEE International Solid-State Circuits Conference

With MTL/I^2L, new circuit/device concepts have been devised to improve power delay and speed limit of superintegrated logic circuits by making stored charge in the switching device. With devices having the required characteristics the feasibility of this new approach has been shown.

11074

Muller, R. (Siemens AG, Munich West Ger.)
CURRENT HOGGING INJECTION LOGIC: NEW FUNCTIONALLY INTEGRATED CIRCUITS. pp. 174-5. 1975 IEEE International Solid-State Circuits Conference

Major drawbacks of the known functionally-integrated circuits are a fan-in of one for a single output I^2L/MTL gate and a relatively large area consumption for CHL gates. A new approach involving functionally integrated logic-Current Hogging Injection Logic (CHIL)-combines the input flexibility of CHL with the performance and packing density of I^2L, and is fully compatible with I^2L circuits.

11075

Cense, A. and van Straaten, J. (N.V. Philips, Nijmegen, Neth.)
A VERTICAL SYNCHRONIZING CIRCUIT FOR TV RECEIVERS USING INTEGRATED INJECTION LOGIC TECHNIQUES. pp. 184-5. 1975 IEEE International Solid-State Circuits Conference

In a TV Transmitter the vertical frequency is digitally derived from the horizontal frequency. To obtain a vertical synchronization which has the same performance as the fly-wheel controlled horizontal synchronization a digital circuit appears practical to generate the vertical sawtooth from the horizontal oscillator. However, such a system is rather complex, so that normal bipolar circuits are much too expensive. The signal processing cannot be optimized in MOS-techniques unless a separate IC is used for the divider. With I^2L this disadvantage can be avoided by combining with conventional bipolar techniques on one chip.

11076

Rodgers III, R.L. (RCA Corp., Lancaster, PA)
A 512 x 320 ELEMENT SILICON IMAGING DEVICE. pp. 188-9. 1975 IEEE International Solid-State Circuits Conference

Charge Coupled Device (CCD) technology has been used to fabricate a high-resolution, low-blooming, 512 x 320 element silicon image device that generates standard 525-line TV pictures. The device uses a unique single-layer doped polysilicon gate structure. This structure maintains the basic simplicity of the original single-layer devices (self alignment of gates, no steps in gate structure causing opens, and single mask level for all CCD gates), but avoids the gap charging problem.

11079

Suzuki, S., Nagahashi, Y., Tanaka, T. et al.
A STATIC RAM WITH NORMALLY-OFF-TYPE SCHOTTKY BARRIER FET's. NEC Res. & Dev., no. 32 pp., 19-25, Jan. 1974. IEEE J. of Solid-State Circuits SC-8, no. 5, pp. 326-32, 1973

A large scale integrated memory with low power consumption and high operating speed has been developed and evaluated. A fully decoded 256-b static random access memory chip was fabricated by using the enhancement-type Schottky Barrier gate FET's, having a threshold voltage of 0.1 V, obtained by ion-implanation. The memory chip was successfully operated with an access time of less than 150 mW/chip. A single power supply of -1.3V and CML input levels are additional features of the memory chip.

11080

Garvin, H.L. (Hughes Res. Labs., Malibu, CA)
HIGH RESOLUTION FABRICATION BY ION BEAM SPUTTERING. Solid State Technol. 16, no. 11, 31-6, Nov. 1973. Kodak Microelectronics Seminar, San Diego, CA, Dec. 11-12, 1972

Ion beam sputtering has proved to be a useful tool for the fabrication of microelectronic, microwave acoustic, and integrated optics components. It has demonstrated the ability to deposit or selectively remove a wide variety of thin film materials, and when coupled with the masking capabilities of photoresist patterns produced either optically, holographically or by electron beam exposure, devices have been fabricated that were not possible by prior art techniques.

11081

Anon.
FIVE-YEAR PLAN GOAL: IMPROVED MECHANISMS FOR IC RELIABILITY. Electronics 47, no. 1, 3 pp., Jan 10, 1974

Faced with a $5 billion annual bill for maintenance of electronic equipment, the Defense Department is starting a major five-year effort through the advanced research projects agency to improve the quality of integrated circuits. The program, called the Advancement of Reliability, Processing, and Automation of Integrated Circuits is managed by the National Bureau of Standards and has been announced in an industry briefing. The effort is being developed with the help of the three services' reliability laboratories.

11082

Segal, E.D. (Matls. Res. Corp., Orangeburg, NY)
NEW GEOMETRY IN SPUTTERING TECHNOLOGY. Solid-State Technol. 16, no. 12, 100-3, Dec. 1973

In early designs of multiple target sputtering systems, the sputtering targets were placed in the same plane under a top plate and substrates were rotated under each sputtering target so materials could be deposited from that target onto the substrates. This article describes a new geometry in which the sputtering target is rotated over stationary substrates. Advantages of the new geometry are described.

11083

Young, L., Bennett, T. and Lavell, J. (Motorola Semiconductor Prod. Inc., Phoenix, AZ)
N-CHANNEL MOS TECHNOLOGY YIELDS NEW GENERATION OF MICROPROCESSORS. Electronics 47, no. 8, 88-100, Apr. 18, 1974

The latest microprocessor chips are faster than p-MOS devices and handle many more peripherals; often, as in Motorola's M6800 family, a CPU chip will come in a matched set of memory and input and output chips simplifying system production.

11084

Altman, L.
SEMICONDUCTOR RANDOM-ACCESS MEMORIES. Electronics 47, no. 12, 108-10, June 13, 1974

This survey relates the capabilities of available and soon-to-be available random access memories to the needs of today's memory systems. Design considerations as well as economic factors are discussed.

11085

Patel, H. (Intersil, Inc., Cupertino, CA)
MINICOMPUTER ON A CHIP. 4 pp.

Since the IM6.00 utilizes the complementary MOS technology and recognizes the popular minicomputer instruction set, it will enable the innovative system designer to implement microcomputer based systems including battery operated and portable systems, economically and with considerably less design time.

11088

Carlson, G.A. (Sandia Labs., Shock Response of Solids Div., Albuquerque, NM)
A TECHNIQUE FOR TESTING THE TENSILE STRENGTH OF THERMOCOMPRESSION BONDS.
Rept. no. SLA-74-0093, 19 pp., Mar. 1974, AT(29-1)-789

A technique is described for testing the tensile strength of thermocompression bonds using a stress waves generated by pulsed electron beam deposition. The technique has been used to test the strength of bonds prepared using different bonding parameters. Tensile strengths of 1-5 kbar are indicated for the bonds tested.

11089

Charles, T.G. (Försvarets Teletekniska Lab. Stockholm, Sweden)
PRESENT-DAY STATUS OF ACCELERATED TESTING OF INTEGRATED CIRCUITS. Rept. no. ESRO-CR-169, Interim Rept., 84 pp., Jan. 1974. ESTEC Contract no. 609/68

This report covers monolithic and hybrid integrated circuits in general as well as discussing results of accelerated testing and failure modes and mechanisms. It is limited to the literature available at the time of its preparation. This report suggests that screening be substituted for accelerated testing, the resultant failures being subjected to a careful failure analysis. Data on the accelerated testing of hybrid circuits was non-existent. Some results are available from testing of some elements used in hybrid circuits, mainly resistors.

11090

Boffé, G. Pécriaux, G. and Plumat, E. (Laboratoires de Recherches, Contrôles et Applications, Glaverbel, Gilly, Belg.)
FORMATION OF BUBBLES DURING DEVITRIFICATION AND REMELTING OF CRYSTALS IN GLASS.
pp. 47-54. Symposium on Nucleation and Crystallization in Glasses and Melts. 1962

The formation of bubbles during devitrification and subsequent remelting of a soda-lime silicate glass was observed. During devitrification, bubbles formed near high densities of cristobalite crystals in the glass in an oxygen or nitrogen atmosphere, but no bubbles were formed near wollastonite crystals nor when the surrounding gas was water. Possible explanations for these results are presented. During remelting, bubbles evolved under a variety of conditions; the reasons for this evolution are not entirely understood.

11097

Selger, R.L., Wilson, R.G. and Brewer, G.R. (Hughes Aircraft Co., Hughes Res. Labs., Malibu, CA)
BEAM TECHNIQUES FOR FABRICATION OF MICROWAVE INTEGRATED CIRCUITS. Final Rept., Sept. 1970. N00019-69-C-0691

The ultimate goal of this program is therefore to develop the necessary technology to produce micron sized ion beams for implantation doping which can be registered on and deflected over microelectronic circuitry in a programmed manner (i.e., by a computer) so as to form a precision fabrication step not requiring the use of masks. The technology developed is to be compatible ultimately with complete vacuum processing of advanced microelectronics circuits, including high frequency microwave semiconductor devices and integrated circuits.

11098

Keister, F.Z. and Scapple, R.Y. (Hughes Aircraft Co., Culver City, CA)
A THIN-FILM MULTILAYERING TECHNIQUE FOR HYBRID MICROCIRCUITS. Solid State Technol. 17, no. 5, 45-7, May 1974

A novel process for fabricating multilayer thin-film hybrid microcircuits on ceramic substrates is described. The process is simple, economical, and compatible with existing hybrid processing technology. Via holes formed in an organic insulating layer are used to provide electrical through-connections between the top and bottom conductor levels.

11100

Mavor, J. (Inst. of Elec. Engrs.)
M.O.S.T. INTEGRATED-CIRCUIT ENGINEERING.
162 pp., 1973

Chapters

M.O.S.T. Analysis
M.O.S. Technology
Radio-Type Logic
Ratioless Circuit Design
Practical Chip Design Considerations
C.A.D. Techniques
Testing M.O.S.T. Chips
M.O.S.T. Applications

11101

Mobley, R. (Collins Radio Corp., Cedar Rapids, IO)
PROM EXPERIENCE. 2 pp., Jan. 27, 1975

Two different failure modes have been experienced during the program operation (1) The blowing of extra bits. Investigation has shown that this failure mechanism is frequently caused by an internal breakdown of device junctions in the address circuitry which causes the erroneous bits to be addressed. An additional cause for blowing extra bits is due to thermal overstress which is a result of continuous attempts to blow difficult links. These links which are difficult to blow are a result of the suppliers process variations.

11103

Bobbio, A., Ferro, A. and Saracco, O. (Instituto Elettrotechnica Nazionale Galileo Ferraris, Italy)
ELECTROMIGRATION FAILURE IN Al THIN FILMS UNDER CONSTANT AND REVERSED DC POWERING. IEEE Trans. on Reliability R-23, no. 3, 194-202, Aug. 1974

In order to understand better the mechanism of failure due to electromigration in thin metallic films, life tests have been carried out under constant and reversed DC current, by following the changes of specimen resistance till failure is reached. The inversion of the currents is chosen at times which are a decreasing fraction of the specimen life in DC. While under DC current, the resistance of the specimen increases continuously up to failure; when the current is reversed, the resistance decreases to some extent in the first period after inversion, and then increases again, thus showing the partial reversibility of the effect. A large increase in life is observed on specimens in which the current is alternatingly inverted. A model of electromigration damage due mainly to vacancy condensation is presented, in which the behavior of resistance change is derived from the kinetics of void formation.

11104

Dataquest Inc., Palo Alto, CA
LOW POWER SCHOTTKY TTL. Res. Newsletter, 5 pp., Nov. 29, 1974

Low Schottky TTL as one of the most promising new state-of-the-art processes is expected to help determine future market leaders. Low Schottky TTL possesses definite advantages over other logic families--vastly improved product performance, lower manufacturing costs, and greater adaptability to MSI and LSI devices.

11105

Sandia Labs., Hybrid Microcircuit Eng. Div., Electronic Technol. Dept., Albuquerque, NM)
HYBRID MICROCIRCUIT DESIGN GUIDE
Rept. no. SLA-74-0333, 94 pp., July 1974

This design guide describes the thin-film hybrid microcircuit technology available at Sandia, provides guidelines and constraints for laying out a hybrid microcircuit, and describes how to obtain model hybrid microcircuits from Sandia's prototype facility.

11109

Lusher, K.G. and Smith, W.E. (Owens-Ill., Inc., Consumer and Tech. Prod. Div., Toledo, OH)
ADVANCES IN SOLDER GLASS TECHNOLOGY. PART I. CRYSTAL STUDIES. PART II. LOW EXPANSION GLASSES FOR SEALING TO FUSED SILICA. Reprinted from the Proceedings of the Eleventh Symposium on the Art of Glassblowing. 1966

In summary, then, these new solder glasses offer the possibility of sealing fused silica parts together at temperatures which assure that even the finest optical members will not warp. Low stress hermetic seals can be made which are useful at least to the annealing temperature of the solder glass. Demonstrations of flame sealing and furnace sealing with an RF generator as heat source will be carried out during the work shop sessions.

11122

Peck, D.S. and Zierdt, C.H., Jr. (Bell Labs. Allentown, PA)
THE RELIABILITY OF SEMICONDUCTOR DEVICES IN THE BELL SYSTEM. Proc. of the IEEE 62, no. 2, 185-211, Feb. 1974

The history of reliability of semiconductor devices in the Bell System is a story of sequential application of principles: (1) Reliability-enhancing processing principles, which are applied in the absence of completely knowledgeable design and testing control. (2) Testing control principles which follow growing knowledge of process defects and their susceptibility to exposure by test. (3) Design-control principles, which derive from mature processing and the essentially automatic elimination of workmanship defects. These principles were generally applied to the design and reliability technologies of successive decades of semiconductor-device manufacture.

11123

GOMAC
1972 GOVERNMENT MICROCIRCUIT APPLICATIONS CONFERENCE DIGEST OF PAPERS. Sponsored by Dept. of Defense (Army, Navy, Air Force), NASA, Dept. of Commerce (Environmental Science Services Administration and Bureau of Standards), Post Office Dept. and Defense Supply Agency. San Diego, CA, 441 pp., Oct. 10-12, 1972. AD 751 316

Contents:

11124

Thomas, R.W. (U.S. Air Force, RADC, Griffiss AFB, NY)
IC PACKAGES AND HERMETICALLY SEALED IN CONTAMINANTS. pp. 31-6. 1972 Government Microcircuit Applications Conference

An extensive analysis of gas in integrated circuit packages has revealed a lack of adequate control by the semiconductor industry. Contamination mechanisms, gas analysis procedures, fine and gross leak test inadequacies, and specification recommendations will be discussed.

11125

Grossman, N.J. and Heid, K.K. (Northrop Corp., Electronic Div., Navigation Dept. Hawthorne, CA)
BLIP$_{TM}$-BEAM LEADED INTERCONNECT PACKAGING. pp. 37-50. 1972 Government Microcircuit Applications Conference

This paper describes a microcircuit packaging approach which eliminates flying wire bonds, a major failure mode in microcircuits, and utilizes beam leads formed independently from the active devices. Both intra- and interconnections are made with beam leads thereby eliminating all flying wire bonds. BLIP$_{TM}$ is a multilayered micropackaging concept that is keyed to a disciplined system of component management, interconnection requirements that include integral beam leads, assembly processes and testing of the in-process or completed functional circuit.

11126

Laermer, L. (Singer Co., Kearfott, Div., Little Falls, NJ)
A UNIVERSAL PACKAGING SYSTEM AS APPLIED TO THE ALL APPLICATIONS DIGITAL COMPUTER. pp. 51-71. 1972 Government Microcircuit Applications Conference

A universal packaging system is described which will serve the requirements of military and space electronics during the latter part of the decade. Design features and fabrication techniques associated with the All Applications Digital Computer building block module and its zero force Cam operated connector are highlighted. In addition, the design of the higher level package, which retains a multiplicity of modules, is covered.

11127

Burgess, J.F., Neugebauer, C.A. and Sigsbee, R.A.
EFFECTS OF HIGH ENERGY PULSES ON HYBRID CIRCUIT MATERIALS. pp. 103-6. 1972 Government Microcircuit Applications Conference

The thermal and mechanical behavior of Au, Cu, Al and Ni-Cr films and Al-30% Ge solder on BeO and Al_2O_3 substrates when exposed to a short high intensity energy pulse is examined. A range of energies is considered.

11128

Perschy, J.A. (Johns Hopkins U., Appl. Phys. Lab., Silver Spring, MD)
A GENERAL PURPOSE COMPUTER FOR SATELLITE APPLICATIONS. pp. 166-79. 1972 Government Microcircuit Applications Conference

The computer reviewed in this digest is the third generation digital system for the Navy Navigation Satellites. The first generation system was first launched in 1962 and consisted of core diode circuitry used to perform logic and drive a 50 mil core memory array. The second generation system was first launched in 1966 and consisted of a special purpose processor designed with series 51 RCTL and a 30 mil core memory array driven with hybrid circuits.

11129

Caruso, S. (NASA, Marshall SFC, Huntsville, AL) and
Stahler, M. (GE Co., Space Systems Operation, King of Prussia, PA) and
Schultz, W. (GE Co., Aerospace Electronic Systems Dept., Utica, NY)
DESIGN OF POWER HYBRID MICROCIRCUITS FOR HIGH RELIABILITY APPLICATIONS. pp. 187-90. 1972 Government Microcircuit Applications Conference

In anticipation of the use of power hybrids (>25 watts) on the Space Schuttel, NASA awarded a study contract (NAS 8-26383) to develop guidelines for the design, fabrication, and screening of power hybrid circuits. The material presented in this paper is a summary of the results of that study.

11130

Meacham, J.H. (Westinghouse Elec. Corp., Def. and Electronic Systems Center, Baltimore, MD)
SUBMINIATURIZATION OF TELEVISION CAMERAS THROUGH HYBRID I.C. TECHNOLOGY. pp. 191-202. 1972 Government Microcircuit Applications Conference

Significant advances in performance capability through new sensor developments, as well as improvements in physical format through solid state techniques have been achieved over the past decade. However, television systems, like the majority of other hardware areas, have not kept in stride with the rapidly emerging Multichip Hybrid Package concepts. In an attempt to rectify this situation, a series of subminiature television cameras have been developed which effectively mate the state-of-the-art capabilities in both sensor and hybrid I.C. techniques.

11131

Orndorff, R.M. and Walker, K.R. (Hughes Aircraft Co., Culver City, CA)
RADIATION CHARACTERISTICS OF HARDENED DIGITAL IC FAMILY. pp. 203-08. 1972 Government Microcircuit Applications Conference

This paper presents the radiation characterization in simulated nuclear environments of pilot production units from a recently developed family. The devices were developed by the Air Force Material Laboratory, Wright Patterson AFB, Ohio, and were monolithic integrated circuits designed for use in radiation environments. The technologies utilized in development of these devices included dielectric isolation, thin film nichrome resistors, minimum transistor geometry, photocurrent compensation and resistor current limiting. A total of ten device types were fabricated including six different gate structures, three different bistable multivibrators and a monostable multivibrator. A total of 310 devices were received for this parts characterization program.

11132

Gray, R.M. and Skogmo, D.G. (Sandia Labs., Albuquerque, NM)
UNIVERSAL DIGITAL INTEGRATED CIRCUITS. pp. 209-17. 1972 Government Microcircuit Applications Conference

The universal digital integrated circuit is a radiation-tolerant, beam-leaded design capable of forming with appropriate external pin interconnections any one of four digital circuits.

11133

Gray, R.M. and Petty, T.D. (Sandia Labs., Albuquerque, NM)
RADIATION TOLERANT GATED VIDEO AMPLIFIER. pp. 218-25. 1972 Government Microcircuit Applications Conference

The circuit described is a radiation tolerant, gated, differential video amplifier. The amplifier is an all PNP design realized in monolithic integrated circuit form, featuring dielectric isolation, thin film resistors, and gold beam leads.

11134

Feryszka, R. and Kalish, I.H. (RCA-SSTC Somerville, NJ)
RADIATION RESISTANCE OF COS/MOS CIRCUITS MADE WITH Al_2O_3: SiO_2 GATE DIELECTRICS. pp. 226-32 NAS8-26311. 1972 Government Microcircuit Applications Conference

COS/MOS Logic Circuitry with its low power requirements, high noise immunity and high reliability is of special interest in satellite electronics. This is even more true if COS/MOS circuitry can be made immune to extremely hostile radiation environments.

11135

Huntington, R.C. and Cho, S. (Motorola Inc., Central Res. Labs., Semiconductor Prods. Div., Phoenix, AZ)
UHF HYBRID INTEGRATED 45-WATT TWO-STAGE AMPLIFIER WITH OCTAVE BANDWIDTH. pp. 259-70. 1972 Government Microcircuit Applications Conference

Design and realization of a hybrid integrated 45 watt two-stage-UHF amplifier with 12-16 dB gain over an octave bandwidth are described. Emphasis is on computer-aided design and layout and assembly contributing to low-cost production.

11136

Roberge, J.K. (MIT, Cambridge, MA) and McGonagle, W.H. (MIT, Lincoln Lab., Lexington, MA)
AN INTEGRATED INTERMEDIATE-FREQUENCY AMPLIFER LIMITER. pp. 271-7. 1972 Government Microcircuit Applications Conference

The design and fabrication of an integrated intermediate frequency amplifier-limiter is described. The low power consumption ideally suited for use as part of a communications satellite F-M repeater. Experimental results are presented.

11137

DiBartolo, J., Ince, W.J. and Temme, D. H. (MIT, Lincoln Lab., Lexington, MA)
A HYBRID INTEGRATED FERRITE PHASE SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS. pp. 278-87. 1972 Government Microcircuit Applications Conference

A hybrid integrated driver circuit for latching ferrite phasers is described. Test data on prototype drivers demonstrates ability to control phase accurately over a wide temperature range, interchangeability, and small sensitivity to phaser parameter variations.

11138

Williams, J.D. and Skogmo, D.G. (Sandia Labs., Albuquerque, NM)
DIAMOND: A NEW APPROACH TO MICROELECTRONIC CIRCUIT DESIGN. (Dielectrically Isolated Arrays of Monolithic Devices) pp. 289-96. 1972 Government Microcircuits Applications Conference

DIAMOND is an approach to microelectronic circuit design which reduces many of the problems associated with the design and procurement of radiation-tolerant integrated circuits. Building block standardization is achieved while allowing special purpose circuits, when required.

11139

Shamash, M.B., Lindberg, F.A., Marriott, C.L. et al. (Westinghouse Def. & Electronic Systems Center, Systems Dev. Div. Baltimore, MD)
FLEXIBLE MULTILAYER INTERCONNECTION USING EVAPORATED ALUMINUM CANTILEVERED BEAMS. pp. 297-306. 1972 Government Microcircuit Applications Conference

A compatible multilayer interconnection system including the formation of cantilevered aluminum beams for interconnection of standard chips or very large LSI wafers is described. This packaging technique has all the advantages of an all-aluminum system with the possibility of semi-automation.

11140

Roberts, R.P. (Sandia Labs., Albuquerque, NM)
ONE-MIL GOLD WIRES IN HIGH ACCELERATION HMC APPLICATIONS. pp. 307-26. 1972 Government Microcircuit Applications Conference

Results of an evaluation of one-mil gold wires as used for intraconnections in hybrid microcircuits for high acceleration artillery shell applications are reported. Wire orientation and length control are necessary for successful use in this environment.

11141

Carbajal, B.G. and McMahon, W.R. (Tex. Instr. Inc., Dallas, TX)
ENGINEERING STUDY OF DEVELOPMENT OF TWO LEVEL ANODIZED AL INTERCONNECTS FOR MSI AND LSI. pp. 327-31. 1972 Government Microcircuit Applications Conference

This study covers the process development for two-level anodized aluminum interconnects suitable for LSI integrated circuits, included in this study is a reliability evaluation and a comparison with conventional two-level aluminum interconnect systems. Results of this study have opened the way for the development of a multilevel aluminum interconnect system that is free from problems. Al anodization is a conversion process yields a monolithic conductor-insulator system that is basically flat and does not suffer from the deficiencies incurred in conventional aluminum silicon oxide multilevel interconnect systems.

11142

Davies, D.E. and Roosild, S. (U.S. Air Force, L.G. Hanscom Field, Air Force Systems Command, Cambridge Res. Labs., Bedford, MA)
DEVICE IMPLICATIONS OF ION IMPLANATION DAMAGE IN SILICON. pp. 341-3. 1972 Government Microcircuit Applications Conference

Thermal stimulated current and diode recovery measurements are presented for ion implanted silicon. The results are used to evaluate device possibilities such as bipolar transistors and hyperabrupt diodes where control of implantation damage is critical. Ion implanation offers a doping method that promises to extend the current state-of-the-art of both discrete devices and integrated circuits. The advantages of the precise control attainable over the total dopant dose introducted together with the extreme uniformity in both depth of penetration as well as laterally over an entire wafer surface are immediately apparent. The greatest concern over the applicability of the process centers on the radiation damage that is introduced and how well it can be annealed.

11143

Trepp, R.M. (Westinghouse Elec. Corp., Baltimore, MD)
LOW-POWER CMOS MASS MEMORY. pp. 401-11. 1972 Government Microcircuit Applications Conference

A mass memory of 10^7 bits can be built that is random access, low power, 1.2 microsecond read or write, low size and weight and that would be suitable for airborne radar data memories and for the replacement of space tape recorders. The technology selected in 1970 for the mass memory was complementary metal oxide silicon (CMOS) because of its availability and low power dissipation. Other technologies evaluated were P channel MOS, N channel MOS, and bipolar, but each was found to dissipate considerably more power. Metal nitride oxide silicon (MNOS), change coupled devices (CCD) and orthoferrites (Magnetic bubbles) were considered very promising, but they are in the development stage and unavailable in quantity.

11144

Lodi, R.J., Wegener, H.A.R. and Moberg, W. (Sperry Rand Res. Center, Sudbury, MA)
A 1280-BIT MNOS RAM. pp. 413-19. F33615-70-C-1306. 1972 Government Microcircuit Applications Conference

This paper describes the development of a fully decoded 1280-bit random access memory chip utilizing variable threshold MNOS transistors as the storage elements. The voltage polarity requirements led to the development of a unique control circuit. Chip organization, layout and other design considerations are discussed as well. Finally, test results from fabricated circuits are presented.

11145

Mavity, W.C. (No. Am. Rockwell Electronics Group, Anaheim, CA)
BUBBLE MEMORY STATUS AND TRENDS IN U.S. GOVERNMENT DATA STORAGE APPLICATIONS. pp. 420-26. 1972 Government Microcircuits Application Conference

The usage of bubble memories in the various data storage missions of the sponsoring agencies will be discussed from the standpoint of the present status of U.S. Government/NREG contracts. Projections of availability that can be used to plan future programs are presented.

11146

Zbriger, R.A. (Litton Systems, Inc., Data Systems Div., Van Nuys, CA)
AN LSI MEMORY SYSTEM FOR MILITARY MAINFRAME APPLICATIONS. pp. 427-37. 1972 Government Microcircuit Applications Conference

A random access memory system utilizing 1024 bit dynamic MOS devices has been developed. The system described is nonvolatile, organized 8K words by 33 bits, and meets the requirements of an existing military system.

11147

Livesay, W.R. (Radiant Energy Systems, Newbury Park, CA)
INTEGRATED CIRCUIT PRODUCTION WITH ELECTRON BEAMS. J. of Vacuum Sci. & Technol. 10, no. 6, 1[illegible]-32, Nov.-Dec. 1973

This paper describes the electron optical aspects of two production-oriented electron-beam systems: the electron-beam mask generator for production of integrated circuit masks and an automated electron projection system for mask-to-wafer alignment and exposure. The single electron-beam mask generator employs a field emission source and the performance advantages and disadvantages of this source for microfabrication are detailed. The electron projection system utilizes [illegible]ial magnetic and electrostatic fields to focus the electron image of the integrated circuit photocathode mask onto the silicon wafer. Electron optical aspects of this system are described as well as alignment accuracies achieved.

11148

Ruehli, A.E. and Brennan, P.A. (IBM, Thomas J. Watson Res. Center, Yorktown, Heights, NY)
ACCURATE METALLIZATION CAPACITANCES FOR INTEGRATED CIRCUITS AND PACKAGES. IEEE J. of Solid-State Circuits SC-8, no. 4, 289-90, Aug. 1973

The parallel-plate formula is widely used by the solid-state circuit designer to estimate capacitances in integrated circuits. Since considerable errors may result from using this approximation, this correspondence gives correction curves for a wide range of parameters. It is shown that the finite conductor thickness may significantly contribute to the increase in capacitance.

11149

Anon.
EPOXY VS EUTECTIC BONDING: A STICKY QUESTION. Microelectronics Times, p. 10, Apr. 3, 1975

Some years back MIL-883 dealt epoxies for bonding hybrids a staggering blow by limiting their use in military systems. Since then, rising costs of raw materials and the ascendancy of commercial uses for hybrid assemblies have forced the industry to question the validity of arguments for and against epoxies. The epoxy versus eutectic controversysurfaced again recently at a technical chapter meeting of the International Society for Hybrid Microelectronics. Questions as to the fears or favorings of epoxies were speculated upon.

11157

Schneider, W.C. and Hollingsworth, R.J., (RCA Labs., Princeton, NJ)
DESIGN, PROCESSING AND TESTING OF LSI ARRAYS FOR SPACE STATION. Rept. no. NASA-CR-120224, Rept. no. PRRL-74-CR-41, Quart. Tech. Rept. no. 13, Jan. 1-Mar. 31, 1974, 15 pp., May 1974. N74-32203. NAS 12-2207

The objective of this research program continues to be the development of a low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM) with beam leads. Support has previously been made available to develop an aluminum-gate current-sense version and a silicon-gate voltage-sense version of this memory. Both types of devices performed very well, which resulted in the present effort to make a silicon-gate unit with beam leads. The beam lead process on bulk silicon wafers is fairly well standardized, but not easily transferred to silicon-on-sapphire (SOS). Beam-lead process development on SOS is discussed, and initial electrical results on beam-lead SOS TA5388 devices are presented. A comparison of the beam-leaded 256-bit RAM (TA6567) layout is made with the non-bear-leaded version (TA6473).

11158

1975 IEEE INTERCON CONFERENCE RECORD. SESSION 36. COMPONENT INFANT MORTALITY--CAUSES AND CURES. Sponsored and organized by the IEEE. IEEE International Convention and Exposition, New York Coliseum/Hotel Americana, NY, Apr. 8-10, 1975

Contents:

11159

Fischer, R.D. (Continental Testing Labs., Inc., Fern Park, FL)
ANALYSIS OF ELECTRONIC COMPONENT SCREENING PROGRAMS. 1975 IEEE Intercon Conference Record. Session 36. Component Infant Mortality--Causes and Cures

During the past year, Continental Testing Labs., Inc. participated in a broad variety of testing programs which included approximately 1300 lots of electronic components totaling some 3.16 million devices. The latter period is of particular interest since substantial amounts of information were collected in a computerized data base facilitating a rigorous analysis. Included in the collected data are details of the test programs including results of individual lots. Data collection and analysis began in March and this presentation will focus on the testing of components over the period ranging from Mar. 1-Nov. 30, 1974. Analysis of the available test data was made and conclusion drawn regarding the effectiveness and impact of various screening steps. The bulk of the data relates to commercial and industrial screening. Approximately 10% relates to military test programs.

11160

Mirth, L.A. (IIT Res. Inst., Reliability Analysis Center, RADC, Griffiss AFB, NY)
SCREENING PROGRAM EFFECTIVENESS. F30602-73-C-0065. 1975 IEEE Intercon Conference Record. Session 36. Component Infant Mortality--Causes and Cures

This paper attempts to provide a general means of evaluating a screening program's effectiveness which utilizes terminology appropriate to product management decisions. A benefit/cost model utilizes information developed by Marketing, Manufacturing and Reliability Engineering to estimate the total impact of a screening program and provides a quantitative basis for decision making.

11161

Augustine, A. (Hewlett-Packard, Corporate Quality Assurance Info. Systems, Palo Alto, CA)
HEWLETT-PACKARD FIELD FAILURE DATA BANK. 1975 IEEE Intercon Conference Record. Session 36. Component Infant Mortality--Causes and Cures

This paper describes the computerized systems employed at Hewlett-Packard for the storage of historical field failure data and its analysis. Primary purpose of this presentation is to focus attention on the advantages of maintaining a common data bank. Theoretical and sophisicated mathematical aspects of reliability often required in analysis of failure statistics has been purposely omitted.

11162

Charles, T.G. (Försvarets Teletekniska Lab., Stockholm, Sweden)
A RE-APPRAISAL OF R.A.C. REPORT TM72-1 MICROCIRCUIT WIRE BOND RELIABILITY. FTL C-Rept. no. A16:49, 12 pp., Aug. 1974

This re-appraisal is based on RAC TM72-1, Microcircuit Wire Bond Reliability, covering the reliability of wire bonds in microcircuits. The subject matter has a close affinity to the study of stress models in integrated circuits, presently being carried out by aid of a grant from Styrelsen för Teknisk Utveckling (Swedish Board for Technical Development), Stockholm. The early hopes that TM72-1 could be used directly in this connection were not fulfilled because of certain discrepancies in the presentation of the results. The object of this report is partly to discuss these discrepancies and partly to attempt to re-work the original basic data.

11169

Internatl. Production Technol., Sunnyvale, CA)
TESTING IC'S AT HIGH TEMPERATURES Electronics 47, no. 3, p. 136, Feb. 7, 1974

Production-type handler permits rapid checkout of MOS RAMs and other circuits in DIPs to spot failure modes in high-density applications.

11170

Anon.
FIRST OXIDE-ISOLATED C-MOS CIRCUITS CUT CHIP AREA BY ONE-THIRD. Electronics 47, no. 1, 33-5, Jan. 10, 1974

Fairchild's Isoplanar process promises full C-MOS capability and could lead to C-MOS LSI devices.

11179

Khajezadeh, H. and Rose, A.S. (RCA Solid State Div., Somerville, NJ)
RELIABILITY EVALUATION OF HERMETIC INTEGRATED CIRCUITS IN PLASTIC PACKAGES. Paper no. ST-6395, pp. 1-6. 1975 Reliability Physics Symposium Gallace, L.J., Gottesfeld, S. and Ingrassia, J. (RCA, Solid State Div., Somerville, NJ)
RELIABILITY OF TITANIUM/PLATINUM/GOLD-METALLIZED HERMETIC CHIPS IN PLASTIC PACKAGES - THE GOLD CHIP SYSTEM. Paper no. ST-6367, pp. 1-7, Feb. 1975
RCA, Solid State Div., Somerville, NJ
GOLD CHIP LINEAR INTEGRATED CIRCUITS. Rept. no. HGC-920, 4 pp., 1975

Previous studies of the basic failure mechanisms of conventional plastic encapsulated integrated circuits have led to improvements in materials and processes which have yielded two orders of magnitude improvement in reliability. Additionally, it has been demonstrated that, where severe environmental conditions are encountered, enhanced reliability is provided by device surfaces passivated with a silicon nitride dielectric and metallized with a titanium, platinum, gold interconnecting system. Failures associated with gold electroplating under severe humidity-bias conditions are avoided by the deposition of a dielectric layer over the metallization pattern. Subsequent thermal, electrical, and moisture stress testing has confirmed earlier indications that predicted lifetimes greater than 10^7 hours can be anticipated for these types of integrated circuits when they are operated at a maximum rated temperature of 125°C.

11182

Rickers, H. (IIT Res. Inst., Reliability Analysis Center, RADC, Griffiss AFB, NY)
RELIABILITY ASPECTS OF PROM TECHNOLOGIES 1974 RAC Workshop. Rome, NY, Oct. 23-24, 1974

The current trends toward the development of nonvolatile semiconductor memory systems has fostered a great deal of interest in devices such as the programmable read only memory (PROM). The programmalbe read only memory offers the system designer both economic and flexibility advantages over its predecessor, the mask programmed read only memory. Since the PROM devices may be programmed by the user in many desired patterns, it is necessary to maintain inventory of only one device type rather than maintaining several types, each being programmed in a different pattern. While these characteristics offer obvious advantages, the ramifications of such procedures, especially those pertaining to the device reliability, have received limited consideration. Unlike most other semiconductor devices, the programming and subsequent final testing of the PROM's has become the responsibility of the device user. In order to assess the reliability aspects of the PROM technologies it is necessary to examine the characteristics of these devices and the various programming mechanisms which they employ. Areas of investigation which desire consideration include: 1. Device Fabrication, Logic Implementation; 2. Programming Mechanisms; 3. Device Programmability; 4. Failure Mechanisms; 5. Screening Methods; 6. Long Term Reliability Evaluation. These areas are included in the following PROM discussions.

11190

Gray, P.R. and Meyer, R.G. (U. of CA., Dept. of Elec. Eng. and Computer Sci., Electronics Res. Lab., Berkely, CA)
RECENT ADVANCES IN MONOLITHIC OPERATIONAL AMPLIFIER DESIGN. Rept. no. AFOSR-TR-74-1552, Interim Rept., 11 pp., May 1974. AD/A000 379. F44620-71-C-0087. Reprinted from IEEE Trans. on Circuits and Systems CAS-21, no. 3, 317-27, May 1974

The state-of-the-art in monolithic operational amplifier design is surveyed. A set of large- and small-signal performance parameters are defined and discussed. Relationships between the important operational amplifier parameters of slew rate, offset voltage, and unity gain bandwidth are demonstrated. The dependence of settling time upon the fine structure of the open-loop frequency response is discussed and the recent technological and circuit design approaches to the minimization of settling time are reviewed.

11191

Wristen, H.A. (Assurance Technol. Corp., Carlisle, MA)
STUDY OF SOLID ENCAPSULATED MICROCIRCUITS FOR LONG LIFE APPLICATIONS. Final Rept., Dec. 31, 1974. NAS8-30812

This report documents the results of a study of solid encapsulated microcircuits for long life applications. The study consisted of five major activities which provided a comprehensive, well structured evaluation program. These activities were:

- Establish List of Available Solid Encapsulated Microcircuits
- Research Existing Evaluation, Performance, and Reliability Data
- Review Existing Systems that may be Used as an Evaluation Vehicle
- Review System Fabrication Techniques and Materials for Compatibility with Solid Encapsulated Microcircuits
- Define an Evaluation Program that will Demonstrate the Capability of Solid Encapsulated Microcircuits in Long Life Space Applications

11194

GE, Aerospace Electronic Systems Dept., Reliability & Quality Assurance, Matls. & Components, Utica, NY
GENERAL ELECTRIC AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR PRESENTATION. 87 pp., Apr. 23, 1975

Overview of G.E. Utica, semiconductor quality and reliability practices and experiences. Includes highly summarized data on supplier quality, failure rate experience, failure modes and mechanisms, screening results, and advanced components experience.

11195

Leadon, R.E. and Snowden, D.P. (Intelcom Rad Tech, San Diego, CA)
CHARGE TRANSPORT AND POLARIZATION EFFECTS IN DIELECTRICS OF MSI/LSI DEVICES. Rept. no. HDL-TR-064-1, Rept. no. 8046-002, Final Rept., Feb. 1972-July 1974, 56 pp., Sept. 1974. AD/A000 833. N75-18493. DAAG39-72-C-0064

The purpose of the present program was to investigate the magnitude and characteristics of the charge transfer and polarization that occur during an ionization pulse in typical oxide dielectrics used in MSI/LSI devices, especially those used for passivation and separation of multilevel metallizations. Since the main objective of this study was to understand the physics of the processes that occurred in the oxide, the device geometries and materials were selected to facilitate the acquisition and interpretation of the data. All of the devices tested were simple planar capacitors with convenient areas rather than actual MOS devices or overlapping metallizations.

11197

Oxley, T.H. (GE Co. Ltd., Hirst Res. Centre, Wembley, Engl.)
THE APPLICATION OF INTEGRATED CIRCUITS TO MICROWAVE RECEIVERS. pp. A.14.1(I) 1-8. A74-13392. European Microwave Conference. Brussels, Belg., Sept. 4-7, 1973, Stonehedge, Herts., Engl., 1973

The concept and feasibility of hybrid microwave integrated circuits using open microstrip techniques as applied to microwave receivers has been indicated up to millimeter wavelengths. It is clear that MIC sub-assemblies can play a large role in future system requirements for telecommunication, radar and consumer electronic equipment applications. Improved substrate materials, application of advanced thin film techniques, (i.e. better definition and direct incorporation of resistors, capitors, etc.), availability of beam leaded devices, advances in bonding methods, circuit optimization combining different forms of transmission line and low cost environmentally proved encapsulation techniques, will lead to the full realization of the MIC technology potential of low cost, high reliability and small-low weight MIC products.

11198

Dore, B.V., Johnson, Q.A. and Mueller, R.A. (Electron Emission Systems, Inc., Tucson, AZ)
INTEGRATED THERMIONIC CIRCUITS. Rept. no. AFAL-TR-72-252, Final Rept., 97 pp., Aug. 1972. AD 905 645L. F33615-70-C-1816

This report describes the design and the electrical and nuclear radiation testing of a six-bit shift register made with Integrated Thermionic Circuits (ITCs). An introductory description of the technology is provided and the work leading to the design of the shift register is described, which also includes a discussion of passive components and individual ITC devices. The results of the program demonstrate the feasibility of the technology and indicate that ITCs are superior to the semiconductor state-of-the-art for operation in nuclear environments. An ITC equivalent of a general purpose, airborne computer is discussed. The report concludes with a consideration of the areas in which additional effort must be expected to utilize more of the capabilities of ITCs.

11199

Hughes Aircraft Co., Culver City, CA
STRAPDOWN INERTIAL GUIDANCE LSI COORDINATE CONVERTER PHASE IV GUIDANCE DATA PROCESSOR PHASE II. HAC Ref. no. C7804, Final Rept., Jan. 15,1973-Dec. 15, 1974, 129 pp., Dec. 1974. N00019-73-C-0199

The objective of this program was the application of LSI technology to two specific hardware projects: the Guidance Data Processor and the fabrication, and testing of a packaged arithmetic and control unit with associated memory. The objectives of the Coordinate Converter program were to research, design, and manufacture a strapdown inertial guidance system (ATIGS), using state-of-the-art large scale integration (LSI) technology and including the features of pad relocation and single wafer packaging.

11201

Vincoff, M.N. (RCA, Solid State Div., Somerville, NJ) and Schnable, G.L. (RCA Labs., Princeton, NJ)
RELIABILITY OF COMPLEMENTARY MOS INTEGRATED CIRCUITS. IEEE Trans. on Reliability R-24, no. 4, 255-59, Oct. 1975

This paper describes the results of tests of the stability and reliability of complementary MOS integrated circuits. Operating-life tests at 125°C indicated excellent stability of electrical characteristics of both n-channel and p-channel transistors. Over three million device-hours of accelerated-type operating-life tests indicated a calculated failure rate, at a 60-percent confidence level, of 0.08%/1000 hours at 125°C, which corresponds to 0.01%/1000 hours at 55°C or 0.003%/1000 hours at 25°C. Field-usage reliability data on three satellites in orbit indicate a total failure-rate of 0.005%/1000 hours. This field-usage failure rate, based on over nineteen million operating hours with no failures, compares very favorably with operating-life reliability figures. The observed failure rates are compared to other available data on MOS integrated-circuit reliability.

11203

Beadles, R.L. and Rasberry, P.P. (Res. Triangle Inst., Res. Triangle Park, NC)
FABRICATION OF THE VIDEO PROTOTYPE MACHINE. Rept. no. AFWL-TR-71-106, Tech. Rept., May 28, 1970-Aug. 31, 1971, 62 pp. Jan. 1972. AD742 238. F29601-69-C-0147. F29601-70-C-0071

This report describes the design, fabrication, and preliminary evaluation of a test set to be used for visual inspection of integrated circuits (ICs) on the production line. Laser illumination and spatial frequency filtering are incorporated in the test set. The test set operator is thereby presented with an IC image in which defects on the IC surface are enhanced (made clearly visible) and the detailed circuit pattern is suppressed. The IC image is magnified by 50 to 200 times and displayed on a high resolution closed circuit television monitor. Both spatially filtered and unfiltered images are available.

11204

Rosen, D.E. (Raytheon Co., Equip. Div., Wayland, MA)
INTEGRATED SOLID-STATE TRANSCEIVER. Rept. no. ECOM-0121-4, Final Rept., Jan. 22, 1971-Aug. 1973, 100 pp., Jan. 1974. AD920 033L. Rept. no. ECOM-0121-F, Final Rept. May 1973-Oct. 1973, 112 pp., Apr. 1974, AD 919 111L. DAAB07-71-C-0121

The Solid-State Transceiver Module Program is an engineering development effort to produce, design and develop high volume production techniques for an all solid state L-band transceiver. Principal goals are to produce a highly reliable module which will meet all electrical specifications and which can be produced in large quantities at low cost. At various intervals during the program, development progress was demonstrated by fabrication, test, and delivery of feasibility modules, and engineering development modules. At the program conclusion, ten prototype modules were fabricated using production facilities. The updated report presents test plan, test setup procedures and contitions for a 200,000 module hour reliability study of 75 solid state, L-band transceiver modules. Data and results are obtained during the reliability test, along with a failure analysis of the 17 modules which failed.

11206

Dillon, L., Jr. (RCA, Advanced Technol. Labs., Govt. and Com. Systems, Camden, NJ)
RADIATION HARDENED MIS INPUT/OUTPUT SUBSYSTEM DEVELOPMENT. Rept. no. AFAL-TR-74-152, Final Rept., 83 pp., Apr. 1974. AD 920 771L. F33615-72-C-2110

The objective of this effort was to determine the optimum technology for developing a radiation-hardened input/output subsystem compatible with a complete MIS computer system. Specifications for the CPU and 1/0 subsystem were developed on contract F33615-72-C-1545. The main goal of the MIS 1/0 program was to develop an operational amplifier to be used as a building block for an A/D or D/A converter in the 1/0 subsystem. The integrated amplifier must be designed such that it will perform all A/D and D/A amplifier functions such as comparator, output amplifier and buffer amplifier, while operating in a total radiation environment including neutron fluence, ionizing dose rate, and total ionizing dose. An initial task on the program involved a tradeoff study where competing hardening technologies were evaluated. COS/MOS/SOS with Al_2O_3 gate dielectric was recommended as the approach with greatest promise because of design flexibility and proven hardness in digital applications. An extensive electrical characterization of the integrated amplifer was accomplished. The characterization showed the amplifier capable of meeting D/A requirements with a few minor changes. Requirements of the A/D are more stringent in that a 10 μs conversion time is specified as opposed to 100 ms for the D/A. The present amplifier bandwidth is insufficient to meet 10 μs requirements.

11207

Whelan, C. (RCA, Solid State Div., Somerville, NJ)
RELIABILITY EVALUATION OF C/MOS TECHNOLOGY IN COMPLEX INTEGRATED CIRCUITS. Rept. no. RADC-TR-75-62, Interim Rept., May 8, 1973-Sept. 30, 1974, 85 pp., Feb. 1975. AD/A008 524.
Interim Oral Briefing, 45 pp., 1975.
F30602-73-C-0282

The objective of this program is to conduct a study and investigation to determine the basic failure mechanisms associated with C/MOS technology as applied to gates and shift registers. Representative devices incorporating the latest commercially available state-of-the-art technology (as distinguished from development technology) are to be subjected to a series of stress tests for the purpose of evaluating existing reliability screens, developing special screens, and assessing long-term reliability. As a result of this study, the MOS failure rate prediction model is to be updated for C/MOS.

11208

Mazenko, J.J. (Hughes Aircraft Co., Ground Systems Group, Tech. Serv. Group, Fullerton, CA)
RELIABILITY STUDY OF BEAM LEAD SEALED JUNCTION DEVICES. Rept. no. RADC-TR-75-50, Final Rept., Apr. 1973-July 1974, 122 pp., Mar. 1975 AD/B003 569L.
F30602-73-C-0204

Over 4000 beam lead sealed junction devices, of nine different types, both linear and digital and from four different manufacturers, were physically and electrically characterized. The devices were then sealed (in hermetic and nonhermetic packages) and were environmentally stressed under both operating and nonoperating conditions. Performance was determined and failures categorized according to type, class, complexity, manufacturer, package and screen.

11210

GE Aerospace Electronic Systems, Utica, NY
COMPONENT TECHNOLOGY AND STANDARDIZATION. Vol. 1-3, 1974-1975

The components technology and standardization manual is a product of the General Electric Company's Aerospace Electronic Systems Department, a subdivision of Aircraft Equipment Division, located in Utica, New York. The departments's products are all high reliability electronic systems (e.g., radar, minicomputers, etc.) designed for aircraft and space applications. The manual was originated by the Components Engineering unit (under Reliability & Quality Assurance auspices) with the express intent of maintaining a technology baseline among the department's design engineers and to maximize standard part usage. The CTS Manual aims to provide a summary of the current technical knowledge and experiences of the GE/AESD Components Engineering Unit. It is systemetically arranged as a complete and ready reference to data covering the full spectrum of hi-rel electronic component parts. The manual is primarily intended for organizations involved in specifying, procuring, evaluating or using electronic components, especially those involved with military applications.

11219

Raytheon Semiconductor, Moutain View, CA
BEAM LEADS - WHAT ARE THE FACTS?
Raytheon Semiconductor Prod. News, no. 4, Feb. 17, 1975

This newsletter offers a rebuttal to a study by Hughes on beam lead products presented at the 1974 ISHM Conference. (see 11208) Raytheon finds the report which critized device availability and reliability to be invalid and not substantiated by test results.

11222

Shannon, G.W. (U.S. Air Force, RADC, Griffiss AFB, NY)
DEGRADATION OF MONOLITHIC SEMICONDUCTOR DEVICES BY HIGH AMPLITUDE CURRENT PULSES. Rept. no. RADC-TR-75-17, In-House Rept., Jan. 4, 1973-Sept. 30, 1974, 65 pp., Feb. 1975. AD/B002 963L

This report presents the results of an investigation into monolithic semiconductor device beta degradation from nanosecond current pulses. Subjects covered include (1) background information on pulse degradation, (2) experimental results obtained from the study of monolithic semiconductor array overstressing, (3) a model of devices after they have been damaged by pulsing, and (4) methods that can be used to harden against and, in many cases, prevent pulse damage.

11223

Schmitz, G.E. (Sperry Rand Corp., UNIVAC, Reliability Group)
THE FACTS AND FALLACIES OF RADIATION HARD DEVICE SPECS. Evaluation Eng., pp. 10-12, 52, Sept.-Oct. 1969

This evaluation engineering exclusive provides an in-depth review of "radiation hard" specs, including recommendations outlining the data which is desirable in a device spec intended for use in a general radiation environment.

11224

Banks, S.B., McCullough, R.E. and Roberts, E.G. (Tex. Instr. Inc., Dallas, TX)
INVESTIGATION OF MICROCIRCUIT SEAL TESTING. Rept. no. RADC-TR-75-89, Rept. no. TI-03-74-14, Final Rept. Feb. 1973-Aug. 1974, 237 pp., Apr. 1975. AD/B004 618L. F30602-73-C-0150

The purpose of this investigation was to determine the detection ranges of Test Conditions A,B,C and E of Method 1014, Mil-Std-883. Also to examine test variables and modifications of the methods for possible expansion of the detection ranges, and to improve the overall test results. This report discusses the various tests conducted and the results of these tests. In addition to the standard test conditions, various exposure pressures and times of both helium and radioisotope tracer gases are examined. Surface absorption, gettering materials, and controlled orifice helium testing are each examined and discussed. Also the gross leak bubble and weight gain test methods are evaluated for sensitivity and effectiveness using various pressures, pressurization times, and fluids for the purpose of optimizing test conditions and defining reject criteria.

11227

Basile, R.L. and Domingos, H. (Clarkson Coll. of Technol., Potsdam, NY)
CTRUMP: ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCTION HEAT FLOW IN SOLID STATE DEVICES. Rept. no. RADC-TR-75-74, Phase Rept., 145 pp., Mar. 1975. AD/A010 002. F30602-72-C-0463

The TRUMP program, developed by Arthur Edwards of the Lawrence Radiation Laboratory, has been adapted for use on the IBM 360/44, under the name CTRUMP. Modifications were made to enable calculations of three dimensional heat flow in solid state devices, as a result of internal conduction and internal heat generation with constant boundary conditions. CTRUMP was then used to calculate temperature rise in thin film and carbon resistor models, as well as in a model of a gallium arsenide Gunn effect diode. An operating manual for CTRUMP is included as an Appendix.

11228

Anstead, R.J. (NASA, Goddard SFC, Greenbelt, MD)
TECHNIQUES OF FINAL PRESEAL VISUAL INSPECTION. Rept. no. NASA SP-6509, 60 pp., 1975

This text concerns the final preseal visual inspection of microcircuit devices to detect manufacturing defects and reduce failure rates in service. It outlines the processes employed in fabricating monolithic integrated circuits and hybrid microcircuits, discusses various failure mechanisms resulting from deficiencies in those processes, and gives the rudiments of performing final inspection.

11231

NASA, Goddard SFC, Greenbelt, MD and Sperry Rand Corp., Sperry Support Serv. Facility
FAILURE ANALYSIS OF ELECTRONIC PARTS: LABORATORY METHODS. Rept. no. NASA SP-6508, 79 pp., 1975. NAS5-21444

Failure analysis of failed parts is a valuable technique which promotes improved reliability by focusing the design and manufacturing efforts on prevention of the underlying failure causes. Failure analysis techniques and data are also frequently used to analyze candidate parts being considered for new designs or new work where proper performance for extended periods in difficult environments, and at minimum overall cost, is required. Failure analysis of electronic parts requires technical expertise, sophisticated equipment, and much analytical reasoning. Experience plays a large role in the development of such expertise, determination of specific equipment needed, and in the selection of analytic reasoning appropriate to the applications and problems involved. This report documents the methods used in the Parts Analysis Lab. at Goddard.

11232

Tompsett, M.F. (Bell Labs., Murray Hill, NJ)
SURFACE POTENTIAL EQUILIBRATION METHOD OF SETTING CHARGE IN CHARGE-COUPLED DEVICES. IEEE Trans. on Electron Devices ED-22, no. 6, 305-09, June 1975

A method of setting charge in a charge-coupled device (CCD) is described whereby the input diode is suitably pulsed and an amount of charge is retained in a potential well under the first transfer electrode. It is shown that, within limits defined by the operating potentials of the device, the sizes of the generated charge packets are linearly dependent on the voltage difference between the first transfer electrode and the input gate. They are also independent of threshold voltage. The method has important applications in all CCD's where it is necessary to obtain a linear low noise charge input that is uniform from one device to another. The linearity has been demonstrated with a 64-element CCD which with a sinusoidal input shows second and third harmonics to be 40 dB down from the fundamental. Measured rms input noise was above the minimum theoretically achievable value but was still 80 dB down from the peak signal level. The electrode area was 2000/m^2.

11233

Bauer, J., Cottrell, D.F., Gagnier, T. R. et al. (Martin Marietta Aerospace, Orlando Div., Orlando, FL)
DORMANCY AND POWER ON-OFF CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND PART RELIABILITY. Rept. no. RADC-TR-73-248, Final Rept., Mar. 1972-May 1973, 186 pp., Aug. 1973. AD 768 619. F30602-72-C-0243. F30602-72-C-0247

Martin Marietta has conducted two programs to: 1) collect, study, and analyze reliability information and data on dormant military electronic equipment and parts and to develop current dormant failure rates, factors, and prediction techniques. 2) collect, study, and analyze reliability information and data on military electronic systems subjected to power on-off cycling, to correlate failure incidence with power on-off cycling, and to quantify power on-off cycling effects with respect to the dormancy and operating states. This data has been processed and presented in the form of dormant and cyclic failure rates and factors by part types and subtypes for various part classes. Dormancy failure rate and cyclic ratio factor charts have been constructed and partially validated. Environmental effects on the various part classes are discussed, together with factors relating them to one another in other energy states.

11234

Anon.
PROCEEDINGS OF THE TECHNICAL PROGRAM. 1969 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE. 634 pp., Anaheim, CA., Feb. 11-13, 1969, Philadelphia, PA, June 10-12, 1969

Sessions:

I	Thermal Design for Efficient Electronic Equipment Cooling
II	New Connector Concepts and Applications
III	Advanced Manufacturing Techniques - I
IV	Printed Wiring & Multilayer Design & Manufacture
V	Advanced Manufacturing Techniques - II
VI	Connection and Interconnection Techniques
VII	Space Systems Packaging
VIII	Automated Electronic Testing Techniques
IX	Hybrid Microcircuit Processes
X	Packaging Techniques for Underwater Electronic Systems
XI	Chemicals and Materials in Electronic Packaging
XII	Automated Artwork Generation for Printed Circuits & Integrated Circuits

RELIABILITY ENHANCEMENT OF FILM-HYBRID MICROCIRCUITS SESSION

11235

Costello, B.J. (Argus Eng. Co., Hopewell Junction, NJ)
INFRARED HEATING APPLICATIONS IN MICROCIRCUIT ASSEMBLY. pp. 136-43. 1969 NEPCON Proceedings

This paper dwells on concentrated infrared heating and how it has been successfully applied to operations in microcircuit assembly. More important, it is the intention of this paper to emphasize the enormous potential of concentrated infrared and the freedom it gives the process design engineer in solving difficult heating problems.

11236

Kimura, S. (Kamaya Elec. Co., Ltd., Yamato City, Japan)
THICK DIELECTRIC FILM WITH HIGH DIELECTRIC CONSTANT. pp. 404-11. 1969 NEPCON Proceedings

The highest dielectric constant obtainable at present is 5,000 but a higher value can be expected through an improvement of substrate heating and some additives. Experimentally, the value of 6,000 has been obtained. Considering the fine crystalline structure of the film, the value may be raised higher than that of ceramic, but that has not yet been achieved except in the case of using pure barium titanate which has a dielectric constant of 1,500 whereas that of the film produced with it is 3,000 after heat treatment at 1,400°C. Incorporating conventional as well as new concepts in capacitor production into this technique, this film-forming technique will further contribute to microminiaturization of electronic circuits, especially in consumer products because of its low cost and other advantages mentioned previously.

11237

Gifford, R.W. (Tektronix, Inc., Beaverton, OR)
THICK FILM HYBRID INTEGRATED CIRCUITS. pp. 412-19. 1969 NEPCON Proceedings

The rise of the hybrid integrated circuit has been exceptional, due to its flexibility, small size, low tooling costs, high yield through repairability, and inherent ability to withstand severe environmental conditions. As with most new devices, many perplexing challenges are met. The solution of many of these problems are the subject of this paper.

11238

Miller, L.F. (IBM Components Div., East Fishkill Facility, Hopewell Junction, NY)
MODULE MATERIALS FOR CONTROLLED COLLAPSE CHIP JOINING. pp. 432-45. 1969 NEPCON Proceedings

This paper describes the screening materials which were used for demonstrating such processes within the context of IBM's SLT module fabricating equipment[2]. It is directed toward screening operations which, within some limitations of line width, conductivity, and circuit card compatibilities, demonstrate unique advantages of economy, flexibility, and reliability. It discusses the types of screening materials as well as some technical aspects relating to their formulation, limitations, and performance. The following types of materials are discussed: Tinnable lands, Nontinnable Lands, solder stopoffs (dams) and dots.

11239

Zimmerman, D.D. and Hicks, R.E. (Johns Hopkins U., Appl. Phys. Lab., Silver Spring, MD)
PREPARATION OF SUBSTRATES WITH BUMPS FOR FACE-DOWN BONDING OF HYBRID COMPONENTS. pp. 518-28. 1969 NEPCON Proceedings

It is the intent of this paper to report on the processes developed to form several types of bumps on substrates with the hope of bringing some relief from the limited availability of hybrid add-on components with reliable bonding bumps. The techniques described in this paper are considered to be an interim step in the progress of microelectronic hybrids.

11240

Cooley R.L. (Burton Res. Labs., Culver City, CA)
GOLD PLATING THE EFFECT OF THE DESIGN SPECIFICATION. pp. 529-32. 1969 NEPCON Proceedings

The military specs for gold plating are simply a rehash of the rather ancient specs for other types of plating. The specs for cad and zinc and copper and silver were better than nothing when they were written but they make almost no sense in the technology of today. If gold is an important part of the system (and it usually is), the designer should write a specification to cover his end requirements. The reasoning here is simple: the designer knows what his end requirements are, but often does not know the plating parameters necessary to obtain the desired results. The first step, of course, is to decide what attributes are essential, then specify a test which will determine if the plated components possess the required property. In designing the test, the engineer will isolate probable modes of failure. Then he will devise a test to which the failure mode is sensitive. Failure can be due to manufacturing stresses, life stresses or degradation.

11241

Reed, R.A. and Brion, K.J. (No. Am. Rockwell Corp., Autonetics Div., Anaheim, CA)
DETECTION AND CORRECTION OF MATERIALS AND PROCESSES PROBLEMS IN THIN FILM NETWORKS. pp. 597-601. 1969 NEPCON Proceedings

This paper describes the techniques, instrumentation and findings of a failure analysis of products of corrosion discovered in the HTFC. Two methods of corrosion were postulated. 1) Electrolyte ions are transported across a mosit insulator surface by an induced external potential. 2) the potential is developed internally. Hermeticity tests, mass spectrometric techniques and measured silver migration were used to verify the presence of moisture. Infrared spectroscopy was used to determine the presence of organics, emission spectrographs verified the elements found in the microprobe and x-ray diffraction was used to ascertain the compounds. Results of the study were used to develop process and material changes which significantly improved HTFC reliability.

11242

Cole, E.M. and Groves, H.T. (Litton Systems, Inc., Data Systems Div., Van Nuys, CA)
EFFECTS OF BONDING TECHNIQUES ON THE RELIABILITY OF HYBRID MICROCIRCUITS. pp. 602-4. 1969 NEPCON Proceedings

Although the primary consideration in this paper is the reliability of the bonding process itself, several other process factors will be discussed. These factors are directly related to the ability to bond by a particular method, and most of them occur prior to receipt at the hybrid manufacturers' facility. Only three basic types of bonding processes were considered in this study. These are wire bonding, flip chip bonding and beam lead bonding.

11243

Szekely, G.S. (Aerojet Gen. Corp., Azusa, CA)
ALUMINA SUBSTRATED RELIABILITY CRITERIA: A USER VIEW-POINT. pp. 605-31. 1969 NEPCON Proceedings

Certain reliability-oriented information was presented which is believed to be of interest to the film hybrid microcircuit designer, producer, packager, and user. The role of alumina substrates was highlighted, along with details on substrate fabrication methods, checks and controls, selected problem areas, and the special significance of the terms: density, homogeneity, and microstructure. It was shown how the four technical areas of composition, internal texture, crystalline structure, and surface character influence the product's desirable physical and electrical parameters.

11245

Tocci, L.R. et al. (Rockwell Internatl., Electronics Res. Div., Anaheim, CA)
MAGNETIC BUBBLE MEMORY
Rept. no. AFAL-TR-75-75, Final Rept., Jan. 2, 1973-Dec. 31, 1974, 156 pp., May 27, 1975. F33615-73-C-1103

This program concentrated on three major areas of investigation. The first one was a study of the temperature stress/anneal effects on the permalloy thin films that are used for the bubble propagation and detection elements. The second one was the development of bias field temperature compensating techniques using temperature dependent magnets. The third area studies was start-stop which is the operational mode employed for asynchronous operation or in case of power failure. A review of bubble memory package concepts and techniques is given. Also a comparison of several thick and thin chevron bubble sensors is made.

11246

U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Washington, D.C.
SEMICONDUCTOR MEASUREMENT TECHNOLOGY. Rept. no. NBS-SP-400-4, Quart. Repts. no. 22,23, Oct 1, 1973-Mar. 31, 1974, 101 pp., Nov. 1974. AD 775 919

Principal accomplishments during this reporting period include:
1. identification of major problem areas in connection with measuring and inspecting photomasks,
2. development of a mathematical model suitable for interpreting thermally stiumulated current and capacitance measurements on junction diodes and metal-oxide-semiconductor (MOS) capacitors,
3. completion of a preliminary evaluation of a method, based on the transient capacitance voltage characteristic of an MOS capacitor, for measuring thickness of epitaxial layers up to 2μm, and
4. development of criteria for use in nondestructive wire bond pull tests.

Results are also reported on spreading resistance, capacitance voltage, and carrier mobility measurements polynomial fits for energy band gap and hole and electron effective masses in silicon; methods for characterizing oxide films; evaluation of sheet resistance and collector resistor test structures; evaluation of a photoresist spinner test; scanning electron microscopy; bonding of aluminum ribbon wire to thick film copper; bonding of platinum wire to thin film aluminum; leak rate calculations in the transition flow regime; transistor thermal response measurements; and radiation response of microwave mixer diodes.

11247

U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Washington, D.C.
SEMICONDUCTOR MEASUREMENT TECHNOLOGY Rept. no. NBS-SP-400-8, Quart. Prog. Rept. no. 24 Apr.-June 30, 1974, 70 pp., Feb. 1975. AD 775 919

Principal accomplishments during this reporting period include:
1. identification of surface preparation procedures which improve the quality of spreading resistance measurements.
2. preparation of videotaped tutorial discussion of thermally stimulated current and capacitance measurements,
3. completion of an analysis of the apparent position of an opague edge when viewed with incoherent and coherent illumination, and
4. completion of the construction of a flying-spot scanner.

11248

U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Washington, D.C.
SEMICONDUCTOR MEASUREMENT TECHNOLOGY. Rept. no. NBS-SP-400-12, Quart. Rept. no. 25, July 1-Sept. 30, 1974, 59 pp., May 1975. AD 775 919

Principal accomplishments during this reporting period include:
1. completion of all effect measurements to determine activation energies of the gold donor and acceptor levels in silicon;
2. successful direct measurement of fast interface state density with the circular CCD test structure; and
3. demonstration of the feasibility of the use of acoustic emission as a non-destructive means for testing individual beam-lead bonds.

11250

Peattie, C.G., Adams, J.D., Carrell, S.L. et al. (Tex. Instr. Inc., Quality and Reliability Assurance, Semiconductor Group, Dallas, TX)
ELEMENTS OF SEMICONDUCTOR-DEVICE RELIABILITY. Proc. of the IEEE 62, no. 2, 149-68, Feb. 1974

Semiconductor-device quality and reliability are discussed in the context of the major factors producing failures, the relationship of process technology and its control to device quality and reliability, the testing procedures used to determine quality levels, and screening procedures that can be employed to segregate certain levels of device quality. Failure rates are presented for transistors and for both bipolar and MOS integrated circuits in several types of packages and for several kinds of device process technology.

11251

Dierking, W.H. and Bastian, J.D. (Rockwell Internatl., Electronics Res. Div., Anaheim, CA)
SOS/MOS MODELING FOR CIRCUIT DESIGN. 6 pp.

A nonlinear transient model for SOS/MOS transistor design and circuit implementation is described. Variabilities due to operating point and temperature effects are shown. Input data required for the model, and the computerized circuit analysis program (SYSCAP), which incorporates the model, are discussed. A comparison with actual test results is made for an SOS circuit.

11253

Grossman, S.E.
THERMAL DESIGN: PART I. THE THERMAL DEMANDS OF ELECTRONIC DESIGN. Electronic 46, no. 23, 98-101, Nov. 8, 1973
Marshall, S.B. and Dewey, R.F. (Sprague Elec. Co., MA)
THERMAL DESIGN: PART II. PLASTIC POWER ICS NEED SKILLFUL THERMAL DESIGN. Electronics 46, no. 23, 102-04, Nov. 8, 1973

This article discusses thermal design considerations for ICs. Techniques discussed in part one include device arrangement on the chip, thermal gradients use of heat pipes and liquid cooling. Part two deals primarily with higher power linear plastic ICs and discusses factors such as thermal impedance use of heat sinks and convection cooling.

11254

Sato, S. and Yamaguchi, T. (Sony Corp., Atsugi Plant, Semiconductor Div., Japan)
STUDY OF CHARGE STORAGE BEHAVIOR IN METAL-ALUMINA-SILICON DIOXIDE-SILICON (MAOS) FIELD EFFECT TRANSISTOR. Solid State Electronics 17, no. 4, 365-75, Apr. 1974

The basic characteristics and charge storage behavior of metal-alumina-silicon dioxide-silicon (MAOS) field effect transistors have been investigated as a function of the oxide thickness. The typical charge storage behaviors have also been measured on devices with SiO_2 films of 50Å and Al_2O_3 films of 700 Å and the results are interpreted in terms of electron and hole transport processes across thin SiO_2 layer and electron injection from Al electrode by tunneling mechanism. In the MAOS structure, the shift of threshold voltage from initial state is within about 23 V and can be reversibly controlled, more than 10^6-times at least, by alternate electric fields under suitable stressing condition. It is considered that the charge storage time is practically infinite at room temperature and of the order of 10^6 hr at 150°C. The failure behaviors of device parameters under the repeated field stressing and cycles can be also accounted for in terms of electron accumulation within Al_2O_3 films and at interfaces between Al_2O_3 and SiO_2 films.

11255

Eaton, S.S. (RCA Solid State Div., Somerville, NJ)
SAPPHIRE BRINGS OUT THE BEST IN C-MOS. Electronics 49, no. 12, 115-20, June 12, 1975

When thin-film silicon on sapphire substrates replaces bulk silicon complementary-metal-oxide-semiconductor technology achieves much better performance; costs should drop as volume rises.

11258

Hunt, J. and Green, A. (Fairchild Camera and Instr. Corp., Syossett, NY)
INTEGRATED MONOLITHIC PHOTOSENSOR ARRAYS. Rept. no. ECOM-72-0214-F, Final Rept., Jan. 1-Dec. 31, 1974, 53 pp., May 1975. DAAB07-72-C-0214

The purpose of this work was to fabricate and optoelectronically characterize 1728 x 1 charge-coupled device (CCD) arrays for use in the tactical page reader application. During this report period the arrays were fabricated and data was taken i.e., transfer characteristic dynamic range, noise equilivent signal, uniformity of photoresponse, and square wave Modulation Transfer Frequency Response. A deliverable 1728 x 1 array device, was operated in a single-lens simulated page reader assembly.

11259

Cricchi, J.R., Blaha, F.C. and Fitzpatrick, M.D. (Westinghouse Elec. Corp., Advanced Technol. Lab., Baltimore, MD)
THE DRAIN-SOURCE PROTECTED MNOS MEMORY DEVICE AND MEMORY ENDURANCE. pp. 126-29. F33615-73-C-1093

The Drain-Source Protected metal-nitride-oxide-semiconductor memory device provides endurance to much greater than $2x10^{12}$ clear/write cycles, eliminates drain or source voltage restrictions during clearing/writing and provides enhancement-mode limited operation. The drain source protected MNOS memory element has been incorporated in a number of LSI arrays, such as the Metering Subsystem and the 2K-bit Block Oriented Random Access memory (BORAM)

11260

Fehr, G.K. (Intel Corp., Assembly and Packaging, Mountain View, CA)
MICROCIRCUIT PACKAGES AND ASSEMBLY TECHNIQUES. PART I. Insulation Circuits 17, no. 11, 37-40, Oct. 1971
PART II, Insulation Circuits 18, no. 12, 16-21, Nov. 1971

The advantages and disadvantages of each package and each assembly technique are discussed. All packages must accomplish certain functions, which are:

1. Chip protection
2. Compatibility with system requirements
3. Mechanical configuration
4. Interface between the die and electronic system
5. Cost objectives

Assembly techniques are covered in this article. Semiconductor assembly is the means by which a circuit is prepared to connect the miniature silicon circuit to an easy to handle package for subsequent operations. General operations in assembly of an integrated circuit are attachment of the circuit (referred to as a die) to the package, performing interconnection from the die to the package, and sealing or encapsulating the package.

11261

Gregory, B.L. and Shafer, B.D. (Sandia Labs., Albuquerque, NM)
LATCH-UP IN CMOS INTEGRATED CIRCUITS
Rept. no. SLA-73-5613, 20 pp., July 1973. N74-12958. 1973 Annual Conference on Nuclear and Space Radiation Effects

The parasitic transistors and pnpn paths present on junction isolated CMOS circuits have been identified and studied quantitatively. Active SCR structures exist which can be triggered electrically or by a radiation pulse. Detailed studies of SCR paths have been performed on two circuits, the CD4007A and the CD4041A, to relate geometrical and materials parameters to latch-up sensitivity. Both normal bias conditions and bias optimum for obtaining SCR action are employed. Several techniques are proposed to eliminate radiation-induced latch-up in future CMOS designs.

11262

Altman, L.
SOLID STATE. Electronics 47, no. 21, 8 pp., Oct. 17, 1974

An increasingly subtle understanding of semiconductor processing techniques, plus a willingness to experiment with new layouts and materials, has brought the solid-state industry to the sophisticated heights of 8-bit microprocessors, 4,096-bit memories, 16,384-bit charge-coupled devices, and linear large-scale integration. What's more, performance and bit densities promise to go right on climbing.

11263

Sequin, C.H. and Mohsen, A.M. (Bell Labs., Murray Hill, NJ)
LINEARITY OF ELECTRICAL CHARGE INJECTION INTO CHARGE-COUPLED DEVICES. IEEE J. of Solid-State Circuits SC-10, no. 2, 81-91, Apr. 1975

The linearity of the electrical signal injection into charge coupled devices has been studied by measuring the generated higher harmonic components of a sinusoidal input. Results obtained with various injection methods and device geometries have been compared. Best results, with all harmonic components more than 40 dB below the fundamental, have been obtained for surface-channel devices with a potential equilibration method in which the signal is applied to a second input gate while the first input gate is held at a dc reference potential. This is true even for reasonably long sampling intervals in spite of an asymmetry of the sampling process with respect to the slope of a time varying input signal, which should theoretically lead to considerable second harmonic distortions. Results obtained with bulk-channel devices are not so good, because of a nonlinear relationship resulting from the changing distribution of the signal charge in the bulk channel.

11264

Hart, C.M., Slob, A. and Wulms, H.E.J. (Philips Res. Lab., Eindhoven, Neth.)
BIPOLAR LSI TAKES A NEW DIRECTION WITH INTEGRATED INJECTION LOGIC. Electronics 47, no. 2, 111-18, Oct. 3, 1974

Using conventional processes, simplified gate structure of I^2L boosts yields and density, while reducing power consumption a thousandfold; the low-cost technique is applicable to both analog and digital circuits.

11265

Muñoz, E., Boix, J.M., Llabres, J. et al. (U. of Madrid, Madrid, Spain)
ELECTRONIC PROPERTIES OF UNDOPED POLYCRYSTALLINE SILICONE. Solid State Electronics 17, pp. 439-46, 1974

Standard semiconductor measurements and techniques have been applied to undoped, high purity polycrystalline silicon to determine its electronic properties. Resistivity and Hall mobility were determined as function of temperature and the ability of polycrystalline silicon to form Schottky barriers and p-i-n junctions has been evaluated experimentally. Present results show Si grain boundaries behaving as p-type layers separating high-resistivity grains, an effective mobility, half the monocrystalline value and an average carrier density in the 10^{15} cm^{-3} range are deduced. A qualitative model is discussed to describe present results.

11266

Thornber, K.K.
THEORY OF NOISE IN CHARGE-TRANSFER DEVICES. Bell System Tech. J. 53, no. 7, 1211-62, Sept. 1974

The noise introduced into charge packets transferred through and stored in charge-transfer devices is calculated in a manner that includes all important relaxation, suppression and correlation effects. This presentation is sufficiently general and detailed that, with a minimum of background in formal noise theory, one can use the approach to evaluate noise in many novel, solid-state devices.

11267

Henderson, R.C., Pease, R.F., Voshchenkov, A.M. et al. (Bell Labs., Murray Hill, NJ)
A HIGH-SPEED P-CHANNEL RANDOM ACCESS 1024-BIT MEMORY MADE WITH ELECTRON LITHOGRAPHY. IEEE J. of Solid-State Circuits SC-10, no. 2, 92-97, Apr. 1975

A switched capacitor, p-channel, 1024-bit random access memory has been made with electron lithography. The basic circuit was the same as that described by Boll and Lynch (in previous papers) but with halved lateral dimensions. The gate length of the switching transistor was 4 μm, and the chip size was required. Even with this modest shrinking of feature size, the minimum access time of the memory was reduced from 100 ns to less than 50 ns.

11268

Change, W.H. and Heller, L.G. (IBM Systems Prod. Div. Lab., Burlington, VT)
STRUCTURE DEPENDENCE OF FREE-CHARGE TRANSFER IN CHARGE-COUPLED DEVICES. IBM J. of Res. and Dev. 18, no. 5, 436-42, Sept. 1974

A detailed numerical analysis of charge-coupled-device charge transfer is described and discussed. The analysis is based on solving the transport equation with a time-dependent surface field calculated from the actual device configuration. Devices with different oxide thicknesses and devices with electrode gaps are examined. The total field is found to play an important role in charge transfer for all cases studied. The effective channel length is modulated by the net field present and is a function of time and electrode configuration. The transfer is found fastest and the effective channel length shortest when the charge is transferred from a region of low oxide capacitance into a region of high oxide capacitance. A low-capacitance electrode gap slows the charge transfer process.

11269

Sony Corp.
POLYSILICON LAYER DOPED WITH OXYGEN IMPROVES DEVICES. Electronics 48, no. 13, 2 pp., June 26, 1975

A polysilicon layer doped with oxygen is being used as a replacement for the conventional silicon-dioxide passivation layer in a wide spectrum of new devices. The products range from bipolar power devices operating at kilovolt levels to low power complementary MOS devices. The same technique is also being used to produce a combination passivation and antireflection layer on high efficiency silicon photodiodes.

11270

Harari, E., Wang, S. and Royce, B.S.H. (Princeton U., Princeton, NJ)
LOW TEMPERATURE IRRADIATION EFFECTS IN SiO_2 INSULATED MIS DEVICES. Rept. no. PSSL 1585 74, 29 pp., May 15, 1974. AD 781 331. N00014-67-2-0151-0034

The storage of positive charge in the SiO_2 insulator of MIS devices has been studied at both 300 and 80K. It has been found that the additional charge stored in the oxide as a result of low temperature X-irradiation behaves quite differently from that induced by room temperature irradiation. This additional charge may be removed from the oxide by photodepopulation techniques, by field emission and by thermal annealing. The charge associated with traps stable at room temperature is shown to be insensitive to these treatments under the same experimental conditions. The experimental data indicate that the observed behavior is not due to positive ion transport within the oxide and strongly indicates that hole transport is occurring. Models for the trapping sites and the role of surface states are discussed.

11271

Berger, J. (Hewlett-Packard Co., Hewlett-Packard Labs., Palo Alto, CA)
NONEQUILIBRIUM PHENOMENA IN ION-IMPLANTED MOS CAPACITORS. Appl. Phys. Letters 24, no. 10, 497-9, May 15, 1974

A new type of nonequilibrium capacitance-voltage characteristic was observed in a particular class of ion-implanted MOS capacitors. A model explaining these characteristics is proposed and a method to use them for evaluation of the implanted layers is suggested.

11272

Kamoshida, M. (Nippon Elec. Co., Ltd., IC Div., Kawasaki-Shi, Japan)
ELECTRICAL CHARACTERISTICS OF BORON-IMPLANTED n-CHANNEL MOS TRANSISTORS. Solid-State Electronics 17, no. 6, 621-26, June 1974

Electrical characteristics, mainly the back-gate bias dependence of threshold voltage and the gate bias dependence of gain term and mobility obtained from ion-implanted n-channel MOS transistors, have been described as a function of implantation dose and transistor dimensions. For comparison, not only specimens implanted through gate oxide but also samples implanted before gate oxidation were measured. Linear dose dependence of threshold voltage was obtained as indicated elsewhere. But deviation from the linearity was observed in a rather lower dose, compared with the p-channel case. Breakdown voltages of n-channel ion-implanted devices have, if any, only a little dose dependence, as determined from p-che devices.

11273

De Troye, N.C. (Philips Res. Labs., Eindhoven, Neth.)
INTEGRATED INJECTION LOGIC-PRESENT AND FUTURE. IEEE J. of Solid-State Circuits SC-9, no. 5, 206-11, Oct. 1974. 1974 International Solid-State Circuits Conference

Integrated injection logic or merged transistor logic incorporating lateral p-n-p transistors as inverters, will be discussed. Speed-power products of 0.13 pJ per gate have been measured in a five-stage closed-loop inverter chain, and packing densities of 400 gates/mm^2 have been achieved. A layout comparison with MOS logic will be presented.

11274

Holmes, F.E. and Salama, C.A.T. (U. of Toronto, Dept. of Elec. Eng., Ontario, Can.)
VMOS-A NEW MOS INTEGRATED CIRCUIT TECHNOLOGY. Solid-State Electronics 17, no. 9, 791-97, Aug. 1974

A new V-groove MOS integrated circuit technology (VMOS) is described. It makes use of preferential etching of silicon to define the channels of the MOS transistors. The fabrication involves either a three or four mask process and is capable of producing either silicon gate or standard metal gate transistors. The technology results in very short channel length devices using non-critical alignment tolerances. Despite the short channel length, the VMOS transistor exhibits lower output conductance and higher breakdown voltage than a standard MOS transistor. Some integrated circuit applications of the technology are also presented, including an R-S flip-flop and a 27 stage bucket brigade shift register.

11275

Darwish, M. and Taubenest, R. (Centre Electronique Horloger S.A., Neuchâtel, Switz.)
C-MOS AND COMPLEMENTARY ISOLATED BIPOLAR TRANSISTOR MONOLITHIC INTEGRATION PROCESS. J. of the Electrochem. Soc. Solid-State Sci. and Technol. 121, no. 8, 1119-22, Aug. 1974

In this work, by using the epi layer with the C-MOS process, the bipolar transistors can be isolated, vs. the non-isolated bipolar transistors provided by conventional C-MOS process. This feature has significant advantages in circuit design. Since the present work was not oriented to a particular circuit application, there was sufficient latitude in optimizing geometry and electrical parameters. It was found that the use of a vertical npn and a lateral pnp transistor design lent itself particularly well to our fabrication process.

11276

Rabbat, N.B. (IBM Corp., Computer Aided Design Lab., East Fishkill, NY)
FEEDTHROUGH IN EMITTER-COUPLED LOGIC CIRCUITS. IEEE J. of Solid-State Circuits SC-10, no. 2, 97-105, Apr. 1975

Emitter-coupled logic circuits transient noise behavior is examined. The mechanisms and causes of feedthrough are analyzed using, first, approximate expressions and, second, an accurate model. The experimental observations of feedthrough give ample evidence of good agreement between the theoretical and computational results. An accurate appraisal of the causes of feedthrough, determine the main factors that offer scope for improvement.

11277

Feldman, C. and Plachy, R. (Johns Hopkins U., Appl. Phys. Lab., Silver Spring, MD
VACUUM DEPOSITED SILICON DEVICES ON FUSED SILICA SUBSTRATES. J. of the Electrochem. Soc. 121, no. 5, 685-88, May 1974

A technique is described for fabricating diodes and MOS devices from vacuum deposited polycrystalline silicon films on insulating substrates. Extremely pure vacuum deposited amorphous silicon films on fused silica substrates were converted into the crystalline phase during device processing. The samples could be converted either during gaseous diffusion of boron or phosphorus at 850°-950 to form n- or p-type layers or during the initial oxidation step at 1000°C in the device definition stage. Film purity was checked by sputter-ion source mass spectrometry. Gaseous diffusion and oxide masking procedures were similar to those used in silicon integrated circuit technology. The quality of the initial resulting planar devices indicates that the process has the potential for producing a variety of silicon devices.

11278

Hynecek, J. (Case Western Reserve U., Cleveland, OH)
HALL EFFECT IN SILICON ON SAPPHIRE. J. of Appl. Phys. 45, no. 6, 2806-07, June 1974

Variations of Hall mobility with gate bias in gated Hall measurements are explained by considering autodoping of silicon from the sapphire substrate. The method of obtaining the true electron Hall mobility for n doped silicon is presented and the conductivity due to the p-type impurities is found.

11279

Bilger, H.R., Tandon, J.L. and Nicolet, M.A. (Ca. Inst. of Technol., Pasadena, CA)
EXCESS NOISE MEASUREMENTS IN ION-IMPLANTED SILICON RESISTORS. Solid-State Electronics 17, no. 6, 599-605, June 1974

The low frequency noise spectra of partially annealed boron-implanted silicon resistors with various geometries are measured. The implantation energies are 50, 80 and 110 keV and the doses are 2.5×10^{12} cm^{-2}, 1.0×10^{13} cm^{-2}. Investigations indicate that the contacts from the implanted layer to the electrode generally contribute small amounts to the total excess noise observed. The excess noise exhibits a strong dependence on the sheet resistance of the layers, while the dependence on substrate bias, implantation energy, and on temperature is relatively weak. A discussion of the results is given in terms of a volume effect. Noise measurements on implanted layers, produced under carefully controlled conditions, show promise as a tool to investigate excess noise.

11280

Thornber, K.K. (Bell Labs., Murray Hill, NJ)
OPTIMUM LINEAR FILTERING FOR CHARGE-TRANSFER DEVICES. IEEE J. of Solid-State Circuits SC-9, no. 5, 285-91, Oct. 1974

A method of filtering analog signals transferred through a charge-transfer device which is capable of greatly reducing the distortion introduced by incomplete charge transfer, is suggested. By using transversal filters consisting in part of single CTD storage cells to achieve the necessary phase delay, the output charge packets can be combined in a manner which offsets the presence of incompletely transferred portions of charge acquired by the packet of interest. The transfer function of the filter is calculated directly from that of the CTD. This further illustrates the importance of treating the operation of CTD's using their transfer function. Examples are given which indicate that in most cases of interest only a few filtering stages are necessary to reduce the distortion to 1 percent of its unfiltered size. Random noise is ignored since it is incomplete charge transfer, which if uncorrected, sets the operational limits of these devices. The method of optimum linear filtering reported here is, therefore, analogous to the method of dynamic detection already reported, which leads to the minimum possible error rates achievable for digital signals in CTD's.

11281

Verway, J.F. and Kramer, R.P. (Phillips Res. Lab., Eindhoven, Neth.)
ATMOS-AN ELECTRICALLY REPROGRAMMABLE READ-ONLY MEMORY DEVICE. IEEE Trans. on Electron Devices ED-21, no. 10, 631-36, Oct. 1974

An adjustable threshold MOS (Atmos) transistor is described that can be used as an electrically reprogrammable read-only memory by changing the charge content of a floating polysilicon gate. This floating gate is charged negatively (write) by means of a nonavalanche mechanism and charged positively (erase) by the avalanche breakdown of source or drain junction and subsequent hole injection into the oxide. The write time is between 10 and 100 ms, the erase time on the order of 1 s. The charge retention of the floating gate is about 90 percent after storage for 1000 h at 125°C.

11282

Bateman, I.M., Armstrong, G.A. and Magowan, J.A. (Queen's U. of Belfast, Belfast, Northern Ire.)
DRAIN VOLTAGE LIMITATIONS OF MOS TRANSISTORS. Solid-State Electronics 17, no. 6, 539-50, June 1974

A comprehensive investigation has been carried out into the factors which influence the maximum drain voltage of an MOS transistor for normal pentode-like operation. The drain voltage is limited by two principal mechanisms, namely punch-through of the drain depletion region to the source, and breakdown, due to impact ionization in the high field region at the drain edge. A two dimensional analysis technique for determining the drain voltage at the onset of either punch through or avalanche breakdown, from a solution of Poisson's equation within the substrate depletion region is described. The solutions are obtained using finite difference numerical methods which take into account the gate-induced potential profiles at the edge of the source and drain junctions. Boundary conditions of zero effective gate bias and channel current are imposed which simplify the solution of Poisson's equation to an electrostatic one. Punch-through and breakdown are discussed for gate bias conditions above and below threshold. The sharp fall in breakdown voltage as the gate bias rises above threshold is explained on the basis of injected charge from the channel into the drain depletion region.

11284

Board, K. (Mullard Res. Labs., Surrey, Engl.)
THERMAL PROPERTIES OF ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT SINKS. Solid-State Electronics 16, no. 12, 1315-20, Dec. 1973

The thermal spreading resistance and temperature-profile properties of a circular semiconductor device mounted on a composite heat sink are considered theoretically. The results are applied to annular and array geometry contacts by the principle of superposition. It is found that considerable reductions in thermal resistance can be achieved which are due both to contact geometry and the composite heat sink. Substantial improvements in the uniformity of the temperature profile in the contact due to the composite nature of the heat sink is also demonstrated and optimum heat sink geometries are illustrated.

11287

Blazek, J. and Blakely, J.N. (Bendix Corp., Kansas City Div., Kansas City, MO)
DEVELOPMENT OF PROCESSES FOR HYBRID MICROCIRCUITS CONTAINING BEAM-LEAD DEVICES. Rept. no. BDX-613-1115, Rev., 156 pp., Aug. 1974. N75-17583. AT(29-1)-613 USAEC

The process-development and proven in work of this program established a complete technology for manufacturing hybrid microcircuits containing beam-lead devices. Previous microcircuits contained chip-and-wire semiconductors. The principal contributions of this work to the existing microcircuit technology were a thermocompression bonding process to bond the gold beam leads and lead frames to the microcircuit substrate and the precision process controls necessary to ensure adequate pull strength on bonds that cannot be nondestructively tested. Other pertinent processes also were refined as needed to provide high microcircuit reliability. These processes and techniques have been released for use in manufacturing seven types of microcircuits for a coded electronic switch.

11290

Sorkin, R.B., Peralta, B.C., Kaiser, D.A., et al. (Battelle Memorial Inst., Columbus Labs., Columbus, OH)
INVESTIGATION AND DEVELOPMENT OF SHORT-TERM TECHNIQUES FOR RELIABILITY MONITORING OF SILICON INTEGRATED CIRCUITS. Final Rept., 136 pp., July 31, 1967. AD 834 680. N62269-3778

The objectives of this contract were to study and further develop accelerated life tests and screening techniques for integrated circuits that are needed, and to analyze the failure of such circuits. A critical portion of the related activity included the study of the circuits and their potential failure modes, the development of failure analysis techniques, and the documentation of suitable procedures for failure analysis. As a result of the study, it was found that the parameters, 1/f noise and harmonic distortion, were correlated with the failed devices. It was further shown that the combined use of these two parameters has promising screening efficiencies. Since these parameters may be relatively independent of the type of circuit under test, they may offer promise for wide-spread application. The ultimate goal of these studies are to provide a cost-effective method in the form of application guide lines and specifications for screening integrated circuits at the equipment manufacturer's plant.

11291

McCaughan, D.V. and Wonsiewicz, B.C. (Bell Labs., Murray Hill, NJ)
EFFECTS OF DISLOCATIONS ON THE PROPERTIES OF METAL SiO_2-SILICON CAPACITORS. J. of Appl. Phys. 45, no. 11, 4928-85, Nov. 1974

The effects of dislocations on the SiO_2/Si interface have been studied at dislocation levels of from 10^4 to 10^9/cm^2. At dislocation levels of 10^6 or less the MOS properties are unaffected; at levels from 10^7 to $10^9/cm^2$ the flat-band voltage increases with dislocation density to the point where it is not measurable at 10^9 dislocations/cm^2, being greater than the SiO_2 breakdown voltage. No effects on the interface state density are seen.

11292

Wonsiewicz, B.C. and McCaughan, D.V. (Bell Labs., Murray Hill, NJ)
ELECTRICAL PROPERTIES OF METAL-SiO_2-SILICON STRUCTURES UNDER MECHANICAL STRESS. J. of Appl. Phys. 44, no. 12, 5476-79, Dec. 1973

Results of three series of experiments in which the electrical properties were measured by MOS capacitance-voltage methods are reported. Stress was applied at the SiO_2-Si interface by deposition of stressed tungsten films. The stress at the SiO_2-Si interface was varied by deposition techniques and heat treatments. The metallization thickness was varied by planar etching and then metallization patterns of widely differing geometries, from 5 to 500 m were used, separately show conclusively that mechanical stresses in the range encountered in device structures do not affect the electrical properties of the SiO_2-Si interface.

11293

Holm-Kennedy, J.W. (U. of CA. School of Eng. and Appl. Sci., Los Angeles, CA)
LONG TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON.
Rept. no. ECOM-0306-73-1, Rept. no. UCLA-ENG-7420, Semiann. Rept., July 1, 1973-Feb. 28, 1974, 39 pp., June 1974. AD 782 255
Rept. no. ECOM-73-0306-2, Rept. no. UCLA-ENG-7511, Semiann. Rept. no. Mar. 1-Aug. 30, 1974, 62 pp., Jan. 1975. AD/A008 045
Rept. no. ECOM-73-0306-3, Rept. no. UCLA-ENG-7550, Semiann. Rept. Sept. 1, 1974-Jan. 31, 1975, 57 pp., Aug. 1975. DAAB07-73-C-0306

Various multivalent dopants were investigated with the goal of obtaining nonvolatile multilevel memory devices in silicon using the field induced trapping (FIT) effect. The test structures included Schottky diodes and resistive bars fabricated in silicon substrates doped with multivalent dopants. Novel device effects were observed and are decribed. A model for a negative differential resistance Schottky barrier oscillator is proposed.

11294

Fresh, D.L. (Aerospace Corp., Eng. Sci. Operations, El Segundo, CA.) and Adolphsen, J.W. (NASA, Goddard SFC, Greenbelt, MD)
SEM EVALUATION OF METALLIZATION ON SEMICONDUCTORS. Rept. no. SAMSO-TR-75-16, Rept. no. TR-0074(4921)-2, 35 pp., June 15, 1974. AD/A004 835. F04701-73-C-0074

A test method for the evaluation of metallization on semiconductors is presented and discussed. The method has been prepared in MIL-STD format for submittal as a proposed addition to MIL-STD-883. It is applicable to discrete devices and to integrated circuits, and specifically addresses batch-process oriented defects. Quantitative accept/reject criteria are given for contact windows, other oxide steps, and general interconnecting metallization. Figures are provided that illustrate typical types of defects. Apparatus specifications, sampling plans, and specimen preparation and examination requirements are described. Procedures for glassivated devices and for multi-metal interconnection systems are included.

11295

Vandre, R.H. (Aerospace Corp., Lab. Operations, Plasma Res. Lab., El Segundo, CA)
PULSED-POWER BURNOUT OF INTEGRATED CIRCUITS. Rept. no.SAMSO-TR-72-226, Rept. no. TR-0073(3124)-1, 33pp., Aug. 15, 1972. AD 752 540. F04701-72-C-0073

Results of pulsed-power burnout testing of the Fairchild 9046 quad dual-input nand gate and the Amelco 6041 dual three-input nand gate showed the circuits to be vulnerable to junction burnout for pulses of less than 100 V and pulse widths on the order of 100 nsec. Calculations based on Wunsch-Bell junction burnout theory showed good agreement with the experimental results. Sample calculations applying Wunsch-Bell theory to integrated circuits are given.

11296

Pieper, W.J. and Pinkus, A.L. (Appl. Sci. Assoc., Inc., Valencia, PA)
COMPUTER GENERATED TROUBLESHOOTING TREES: THE PROGRAM. Rept. no. AFHRL-TR-74-20(II), Final Rept., 96 pp., July 1974. AD 785 139. F33615-72-C-1682

The development of troubleshooting trees by hand for use in job performance aids and other types of maintenance data is a difficult and time consuming process. Development of an effective technology for computer generation of troubleshooting trees will contribute significantly to the development of improved maintenance data. Computer generation of troubleshooting trees will reduce development costs, improve quality control, and provide for systematic consideration of factors which cannot be effectively considered when trees are developed by hand. An early attempt at developing this technology was sponsored by NASA. Procedures and a computer program were developed and used to produce troubleshooting trees for a data flow representation of an electronic system. However, the trees were never tested on actual equipment. The purpose of the project described, in part, in this volume was to update and test the development procedures, the computer program, and the troubleshooting trees.

11297

Fitzgerald, D.J. (IKOR Inc., Burlington, MA)
APPLICATION OF TIME DOMAIN METHODS TO INTEGRATED CIRCUIT SUSCEPTIBILITY. NWL Contractor Rept. no. CR-04-72, Apr. 12, 1972-Feb. 12, 1973, 108 pp., Mar. 12, 1973. AD 909 446. N00178-72-C-0388

A review of the time domain reflection and transmission mode measurement method is presented. The meaning and information content of some time waveforms measured using these methods are discussed. Details of the test fixture structures developed for the susceptibility testing of Flatpack. Dual-In-Line and TO-99 style packages. The test fixture designs allow separate video and microwave signals to be applied simultaneously at each terminal of an integrated circuit. The design method which facilitates the implementation of a matched 50 ohm impedance path to the terminals is discussed and performance data presented. Time domain measurements made on various linear and digital integrated circuits in the test fixtures are described. Data are presented showing the impedance of integrated circuit terminals to injected signals. Fourier transform of a time domain waveform to provide frequency information is dealt with. Experiments performed to determine the susceptibility of selected linear and digital integrated circuits to short pulse interference sources are describe. Susceptibility levels are determined and vulnerable injection points identified.

11298

Vinikman, V., Samual, A. and Schneider, D. (ELTA-Ashdod,Microelectronics Technol., Israel)
SURFACE DESORPTION OF GASES FROM PHOTORESIST. Vacuum 24, no. 2, 77-9, Feb. 1974

This work describes the analysis of gases desorbed in vacuum from photoresists manufactured by Shipley and Kodak, as a function of temperature. Test samples were prepared by spin coating of a special heating element prepared by photolithographic techniques on a nichrome, gold-coated alumina substrate, the degassing of this type of heating element is relatively low by comparison to that of the photoresist. The analysis of gases desorbed was performed at a pressure of 10^{-6} torr utilizing a monopole mass spectrometer. The type of photoresist and temperature were the determining factors in the quantity and species of gases desorbed. In this manner the breakdown temperature of each type of photoresist was determined. The results of this work aid in choosing a photoresist compatible with microelectronic vacuum technology.

11299

Wilson, R.G. and Zimmerman, R.L. (Hughes Res. Labs., Malibu, CA)
MANUFACTURING METHODS FOR IMPLANTATION. Interim Rept. no. 6, Apr. 1-June 30, 1971, 7 pp., July 1971. AD 886-469. F33615-70-C-1238

Work was spent in performing reliability testing of the implantation system and in seeking and eliminating the causes of observed failures or possible long-term weak points. Most of the improvements made were in the electronics and control circuitry areas as these were subjected to longer and more strenuous testing. A radiation survey was made with favorable results. Eleven hours of routine operation (100 keV, 10^{14} ions/cm^2 dose), including five simulated implant cycles, were achieved without any failures other than the failure of the ion source feed line.

11300

Komatsubara, K.F., Narita, K., Katayama, Y. et al. (Hitachi Ltd., Centeral Res. Lab., Kokubunji, Tokyo, Japan) and Kobayashi, M. (Natl. Lab. for High Energy Phys., Oho-machi, Tsukuba-gun Ibaraki, Japan)
TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN n-TYPE INVERSION LAYERS IN (100) SURFACES OF SILICON. J. of Phys. and Chem. Solids 35, no. 6, 723-40, June 1974

In this paper, the detailed characteristics of conductivity of the inversion layer are presented as a function of temperature and carrier concentration, and discussion is made of the scattering mechanism in each range of temperature and carrier concentration, referring to the surfon theory, the coulomb scattering treatment, the effect of carrier freeze-out and also the effect of bound state associated with the ground electric subband.

11301

Nelson, W. (GE, Corporate Res. and Dev., Schenectady, NY)
METHODS FOR PLANNING AND ANALYZING ACCELERATED TESTS. Rept. no. 73CRD034, 21 pp., Mar. 1973

This report is intended to acquaint readers with statistical methods for more effective accelerated tests and data analyses. Briefly surveyed are statistical methods for planning and analyzing accelerated tests where units are subjected to high stresses. Useful results are pointed out that come from these methods, many of which are new, and references are given that explain how to apply these methods. References show how to analyze such data before all test units fail. This important advance makes it possible to terminate a test before all units fail, resulting in savings of time and cost. References also show how to properly analyze data with different failure modes.

11302

Schrottke, G. (IBM Federal Systems Div., Huntsville, AL)
TECHNOLOGY AND FABRICATION SUPPORT FOR THICK FILM MICROELECTRONICS AND PRINTED WIRING BOARDS. Rept. no. DI-S-1800. Rept. no. IBM 74W-00183, Final Rept., 19 pp., June 1974. AD/A004 757. DAAH-01-74-C-0363

The objective of this contract was to provide technical and fabrication services in the areas of thick film hybrid microelectronics and printed wiring boards with the majority of the technical work to be performed in the thick film hybrid area.

11303

Peltzer, D. and Herndon, B. (Fairchild Semiconductor Div., Mountain View, CA)
ISOLATION METHOD SHRINKS BIPOLAR CELLS FOR FAST, DENSE MEMORIES. Electronics 44, no. 5, 52-55, Mar. 1, 1971

Passive isolation promises ICs that combine bipolar speed and MOS density, while simplified masking and a self-alignment feature presage higher yields and reduced costs. These factors could have a far reaching effect in deciding whether MOS or bipolar devices will dominate the development of semiconductor memory technology.

11304

DeFalco, J.A. (Honeywell Info. Systems Inc., Framingham, MA)
COMING UP FAST FROM BEHIND-DENSER BIPOLAR DEVICES. Electronics 44, no. 15, 76-9, July 19, 1971

Because it's now possible to diffuse very thin epitaxial layers, and because new methods of isolating transistors have been developed, bipolar ICs today can achieve MOS component densities. The effort to simplify high-density bipolar integrated circuits continues. None of the techniques described here is the panacea for all circuit fabrication problems, though all represent steps in the evolution of a more efficient bipolar fabrication technique.

11306

Domingos, H. (Clarkson Coll. of Technol., Potsdam, NY) and Anderson, R. (Syracuse U., Syracuse, NY)
AN EVALUATION OF SILICON ON SAPPHIRE TECHNOLOGY. 137 pp.

Silicon on sapphire is a recent microelectronic circuit technology originally devised to eliminate the drawbacks of conventional junction isolation. It has since developed into a high performance MOS-type integrated circuit family. In this report a description of this logic family is given, including such topics as manufacturing processes, device physics, and performance of commercial circuits. The report concludes with an overall evaluation of this technology.

11312

Demizu, K. (Mitsubishi Elec. Corp., Kita-Itami Works, Japan)
DOUBLE EPITAXIAL ISOLATION METHOD FOR THE FABRICATION OF INTEGRATED CIRCUIT TRANSISTORS. J. of Electrochem. Soc.: Solid State Sci. 118, no. 10, 1627-30, Oct. 1971

A new fabrication method is proposed which eliminates the isolation process by introducing a p-type epitaxial layer into the I.C. fabrication process. The typical values of BV_{CEO}, BV_{CBO}, and h_{fe} of I.C. transistors made by this new method are 6.5 - 10V, 16-18V, and 20-60, respectively. This new method is suitable for the fabrication of high-density integrated circuits in view of its simple process and better transistor performance.

11317

Ipri, A. (RCA Labs., Princeton, NJ)
ADVANCED COMPLEMENTARY-METAL-OXIDE-SEMICONDUCTOR CIRCUIT TECHNOLOGY (PHASE I). Rept. no. AFAL-TR-75-48, Final Rept., Dec. 27, 1971-June 30, 1974, 141 pp., May 1975. F33615-72-C-1291

This final report presents the results of a comparison of the silicon-gate double-epitaxial and the silicon gate deep depletion processes. In addition, the fabrication of three test vehicles is discussed: (1) a multipurpose arithmetic building block, (2) a 32 stage correlator circuit, and (3) an 8 x 8 bit multiplier chip. Finally, the development of a beam lead process is presented along with the application of this process to the fabrication of the SOS silicon gate version of the CD4007.

11318

Altman, L.
CHARGE-COUPLED DEVICES MOVE IN ON MEMORIES AND ANALOG SIGNAL PROCESSING. Electronics 47, no. 16, 91-101, Aug. 8, 1974

The structural simplicity of the charge coupled device lowers memory chip costs, while the analog nature of CCD operation is exploited in delay lines, filters, and multiplexers.

11319

Wakefield, R. (Mostek Corp., Carrollton, TX)
PROCESSES FOR MOS IC's. Electronic Packaging and Production 15, no. 7, 169-72, July 1975

The emergence of MOS technology in the semiconductor industry began in the 1960's. The market was slow to accept this technology because of electrical instabilities in the transistors. The MOS explosion was made possible by stabilization techniques that gave the devices the necessary reliability for inherent advantages of high packing densities and ease of fabrication.

11320

Covington, D.W. and Ray, D.C. (GA Inst. of Technol., School of Elec. Eng., Atlanta, GA)
EFFECT OF SURFACE REGIONS ON THE ELECTRICAL CONDUCTIVITY OF EXTRINSIC SEMICONDUCTOR FILMS. J. of Appl. Phys. 45, no. 6, 2616-20, June 1974

Theoretical expressions based on the Boltzmann transport equation, nondegenerate statistics, and Poisson's equation are derived for the electrical conductivity is presented as a function of film thickness and Fuch's scattering indices for the nondegenerate n- p-type semiconducting films. The analysis predicts that the conductivity of thin films having quasisymmetrical space-charge layers at the surfaces should be strongly dependent upon the excess carrier density in these layers even under conditions of specular surface scattering. The limited amount of conductivity data reported for exitaxial germanium films are interpreted using the extrinsic film model. Universal curves are presented for normalized film conductivity as a function of normalized film thickness for accumulated n - p-type films and depleted n - and p-type films having specularly scattering surfaces. The general case analysis yields the symmetrical and flat-band results as previously reported.

11321

Hynecek, J. (Case Western Reserve U., Case Inst. of Technol., Cleveland, OH)
ELASTOREISISTANCE OF n-TYPE SILICON ON SAPPHIRE. J. of Appl. Phys. 45, no. 6, 2631-35, June 1975

Elastoresistance of n-type silicon on sapphire is measured. The measurement is performed with a gated MOS Hall bridge. An extrapolation method is developed to minimize errors due to aluminum autodoping. From the obtained result, it is concluded that the lateral stress present in the silicon causes almost complete depopulation of the energy surface in the k, direction, perpendicular to the surface of the silicon. This in turn causes pronounced changes in the transport properties, such as resistivity or Hall mobility. Qualitative agreement with the theory, in which no scattering mechanism is considered, is obtained.

11322

Mohsen, A.M. and Morris, F.J. (Bell Labs., Murray Hill, NJ)
MEASUREMENTS ON DEPLETION-MODE FIELD EFFECT TRANSISTORS AND BURIED CHANNEL MOS CAPACITORS FOR THE CHARACTERIZATION OF BULK TRANSFER CHARGE COUPLED-DEVICES. Solid- State Electronics 18, no. 5, 407-16, May 1975

The properties of bulk transfer charge-coupled devices may be characterized from measurements obtained using MOS capacitors and field effect transistors. Models are presented for the MOS capacitor and field effect transistor for the case where a shallow doped layer of polarity opposite to that of the substrate is incorporated between the oxide and the substrate. These models explain the observed frequency dependence of the capacitance-voltage characteristics of these devices. Techniques are presented for determining the impurity profile of the buried layer from the low frequency C-V measurements made on MOS transistors. The majority carrier mobilities in the buried layer and at the surface are measured for the BCCD's and compared to the surface minority carrier mobility measured for the surface channel CCD's. Generation lifetimes at the surface, in the buried layer and in the underlying substrate are determined from capacitance-time measurements and leakage current measurements of the MOS capacitors and transistors. Methods are demonstrate whereby the depth from the oxide interface of the potential minmum and its potential can be determined as a function of the various applied biases.

11327

Aharoni, H. (U. of Negev, Dept. of Elec. Eng., Microelectronic Lab., Beer-Sheva, Israel) and A Bar-Lev (Technion-Israel Inst. of Technol., Haifa, Israel)
SOME PRACTICAL REMARKS ON THE DESIGN OF EXPERIMENTAL SYSTEMS FOR EPITAXIAL GROWTH OF Si, Ge AND Si-Ge. Vacuum 24, no. 2, 89-93, Feb. 1974

Epitaxial growth of gpoup IV semiconductors, especially silicon, is an important and very sensitive step in the manufacture of semiconductor devices. The epitaxial layer grows by the addition of atoms to a single crystal substrate in an ordered manner. Any interruption in this order would grow as a fault through many layers and may cause final device failure. The epitaxial system must therefore be designed so as to prevent such faults. Practical considerations concerning a design of an experimental system for growth from the gas phase are described, based on experience gained during its building and operation. The various system components and materials, the necessary instrumentation and system calibration are described. Problems of vacuum tightness of the system and purification of incoming gases are also included. Finally, the basic calculations for obtaining the necessary molar ratios in the reactor chamber so as to achieve the desired layer type and resistivity are reviewed. In the system described, layers of Si, Ge or Si-Ge mixture of desired composition may be grown.

11328

Caruso, S.V. (NASA, Marshall SFC, Huntsville, AL) and Licari, J.J., Perkins, K.L. and Schramm, W.A. (Rockwell Internatl., Autonetics Div., Anaheim, CA)
DESIGN GUIDELINES FOR USE OF ADHESIVES AND ORGANIC COATINGS IN HYBRID MICROCIRCUITS. Rept. no. NASA TM X-64908, Tech. Mem., 66 pp., Dec. 1974. N75-17574
NAS8-26384

A study was conducted to investigate the reliability of organic adhesives in hybrid microcircuits. The objectives of this study were twofold: (1) to identify and investigate problem areas that could result from the use of organic adhesives and (2) to develop evaluation tests to quantify the extent to which these problems occur for commercially available adhesives. Efforts were focused on electrically conductive adhesives. Also, a study was made to evaluate selected organic coatings for contamination protection for hybrid microcircuits. The results of these studies are reported.

11329

Caruso, S.V. (NASA, Marshall SFC, Huntsville, AL) and Honeycutt, J.O. (IBM Corp., Huntsville, AL)
INVESTIGATION OF DISCRETE COMPONENT CHIP MOUNTING TECHNOLOGY FOR HYBRID MICROELECTRONIC CIRCUIT. Rept. no. NASA TM X-64937, Tech. Mem., 52 pp., May 1975

The test program described in this report represents only a summary of the investigations conducted to date on bonding systems for discrete electronic components. Since the use of adhesive in place of soft metals is becoming prominent for high reliability applications, studies to prove this suitability in space-flight avionics hardware were required. In general, adhesives, when selected and properly qualified are acceptable and, in some cases, more reliable, than the traditional solder techniques. Test procedures and qualification criteria are being developed at MSFC and will be proposed as NASA/industry standards for this technology.

11343

McDonnell Douglas Corp., McDonnell Douglas Astronautics Co. East, St. Louis, MO)
INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY - PHASE II.
TEST AND MEASUREMENT SYSTEMS. Rept. no. MDC E1099, 156 pp., July 12, 1974
MOS NAND GATE STUDY. Rept. no. MDC E1101, 53 pp., July 26, 1974
PULSE INTERFERENCE STUDY. Rept. no. MDC E1102, 32 pp., July 12, 1974
PACKAGE EFFECTS STUDY. Rept. no. MDC E1103, 81 pp., July 12, 1974
BIPOLAR NAND GATE STUDY. Rept. no. MDC E1123, 106 pp., July 26, 1974
BIPOLAR OP AMP STUDY. Rept. no. MDC E1124, 78 pp., Aug. 9, 1974
MOS/HYBRID STUDY. Rept. no. MDC E1125, 55 pp., Aug. 9, 1974
SUSCEPTIBILITY SURVEY STUDY. Rept. no. MDC E1126, 83 pp., Aug. 9, 1974.
N00178-73-C-0362

These reports discuss electromagnetic vulnerability assessment studies and results of tests applied to integrated circuits and hybrid devices. The component susceptibility investigations are performed by direct injection of RF energy into the terminals of the device i.e., a hard line connection from the RF source to the component. Package effects are also included. Failure analysis war performed on all failed devices.

11348

Muschinske, J.E., Rangappan, A., Dhaka, V.A. et al. (Fairchild Camera & Instr. Corp., Fairchild Microwave & Optoelectronics, Palo Alto, CA)
SILICON-ON-SUBSTRATE (SOS) INTEGRATED CIRCUIT TECHNOLOGY. Rept. no. AFAL-TR-74-145, Final Rept., Feb. 15, 1973-Feb. 15, 1974, 80 pp., Apr. 1974. AD 923 585L
F33615-73-C-1111

This report describes the work accomplished in research and development program to develop a technology for fabricating high speed bipolar integrated circuits on an insulating substrate. The circuits are fabricated in a thin single crystal silicon film. The insulating substrate consists of a layer of SiO_2 immediately beneath the thin film and a thick polycrystalline silicon support. Complete dielectric isolation is achieved through oxidation of the thin silicon film.

11349

Lane, C.H. (U.S. Air Force, RADC, Griffis AFB, NY)
PRACTICAL PROBLEMS IN THE APPLICATION OF ALUMINUM ELECTROMIGRATION FAILURE STUDIES. 44 pp.

A review of the literature on electromigration research of aluminum thin film conductors is provided as a background for comparison with some real device results on accelerated tests. Issues involved in the application of the research results to specifying current density limits for circuits to be used in military equipments are treated. The conclusions and recommendations suggest courses of action based on the present status of knowledge and practice in aluminum deposition for solid state circuits.

11353

Integrated Circuit Eng., Scottsdale, AZ)
MICROCIRCUIT MANUFACTURING CONTROL HANDBOOK. A GUIDE TO FAILURE ANALYSIS AND PROCESS CONTROL. VOL. I. F30602-74-C0232

The objective of this Handbook is to provide the line engineer, the failure analyst and the solid state research engineer with a concise, up-to-date reference which links the observed failure or yield loss mechanism in an integrated circuit to a specific process induced defect. In a looseleaf format, this Handbook lists the faiure mechanism, its method of detection (i.e., direct analysis or accelerated testing) the processing source, and the means for corrective action. The general aim of the document is to provide precise identification of specific processing defects with definite recommendations for removal using the most sensitive analysis techniques available.

11354

Anon.
PLANAR DIFFUSION SOURCES. Circuits Mfg. 15, no. 9, 54-56, Sept. 1975

Commonly used for chemical deposition applications in the past, gas systems cannot provide close control over sheet resistance values required for semiconductor doping applications. The flow pattern dependence of such systems prevents uniform and repeatable depositions across the wafer and within the run. To get around this problem, some semiconductor makers sacrifice furnace capacity by positioning the slices parallel to the gas flow or horizontal to it. With planar diffusion sources, however, the periodic and alternate spacing of source and silicon wafers along the length of the diffusion boat and perpendicular to the direction of gas flow conserves furnace space and lets each wafer receive an identical and uniform density of dopant. Normal wafer spacing from source wafer to silicon slices ranges from 80-125 mils. For high loading densities, up to 200 manually loaded silicon slices rest back to back in the diffusion carrier.

11355

King. G.
SILICON-ON-SAPPHIRE IC's: TECHNOLOGY FORECAST. Circuits Mfg. 15, no. 9, 4 pp., Sept. 1975

Continually advancing Silicon on Sapphire (SOS) technology offers not only a potential cost competitiveness with bulk-silicon CMOS, but the advantages of high speed, low power dissipation, high packing densities and high reliability. In fact, some devices have demonstrated gate delays of a few nano-seconds and microwatts of power dissipation per gate. Many companies-interested in this technology-are doing research in it and have fabricated devices in the laboratory or on a custom basis. But although SOS seems to be an almost ideal technology, users must resolve some problems before they can exploit SOS in commercial devices.

11357

Hetherington, D.R. (Newmarket Transistors, Ltd., Newmarket, Suffolk, Engl.)
BOND CHIPS WITH CONDUCTIVE EPOXIES. Electronics 23, no. 20, 82-85, Sept. 27, 1975

Epoxies have found wide acceptance for the attachment of active semiconductors, chip capacitors and resistors and other small parts to hybrid microcircuits. Their use gives the designer a high degree of freedom when building complex units, and they allow employment of easily automated processes that provide good yields. Of the three attachment methods currently in use--gold-silicon eutectic bonding soft solder and conductive epoxy--epoxy is the fastest growing technique. This paper will discuss different aspects of epoxy application and properties.

11358

Schaefer, G., Ward, R. and Zakraysek, L. (GE, Aerospace Electronic Systems Dept., Utica, NY)
EVALUATION OF LEAD FINISHES FOR MICROCIRCUIT PACKAGES. Rept. no. RADC-TR-75-171, Final Rept., Jan. 23, 1974-Apr. 23, 1975, 140 pp., July 1975. F30602-74-C-0118

The purpose of this study was to determine the compatibility and effectiveness of surface finishes and undercoats being used on microelectronic package leads. The study was to determine optimum combination of materials and processes, including those in use and those proposed for use, for various lead frame sealing glass combinations. The study covered the actions and interactions resulting from the various process steps the lead materials undergo, from initial rolled sheet condition through the final process of plating to preserve solderability.

11359

IEEE
1973 SYMPOSIUM ON SEMICONDUCTOR MEMORY TESTING. DIGEST OF TECHNICAL PAPERS. Sponsored by the IEEE Computer Society Mideastern Area Committee and the Philadelphia Chapter of the IEEE. Rickshaw Inn, Cherry Hill, NJ , 126 pp., Oct. 2, 3, 1973. IEEE Cat. No. 73 CH0827-6C

Table of Contents

11362

Butcher, D.T., Maddox, H.M. and Neilsen, R.L. (No. Am. Rockwell, Electronics Group, Anaheim, CA)
SURVIVABLE P-CHANNEL METAL-OXIDE-SEMICONDUCTOR (RMOS) COMPUTER DESIGN. Rept. no. AFAL-TR-73-31, Rept. no. C72-446/501, Final Rept., Mar. 20-Sept. 20, 1972, 134 pp., Mar. 1973. F33615-72-C-1732

The significance of this project to the Air Force is the fact that it provides assessment, and develops specifications for employment of advanced radiation hardened field-effect (i.e., Metal Oxide Semiconductor (MOS) and Metal-Nitride-Oxide Semiconductor (MNOS) technologies for military/space computer systems. The characteristics and capabilities of the device and packaging technologies, required for MOS/MNOS computer construction, are defined and compared to the techniques and hardware requirements for long-life computer systems. Specifications are presented for four modular subsystems (CPU, I/O, Memory, and Power Supply) of a minimum demonstration-computer employing radiation hard PMOS/MNOS technologie..

11363

Kmeta, W.J. (SMC Microsystems Corp., Hauppauge, NY) and Nadan, J.S. (U. of the City of N.Y., New York, NY)
THEORY AND PRACTICE OF MOS PROCESSING TECHNIQUES 1973. IEEE Trans. on Mfg. Technol. MFT-2, no. 2, 37-49, Dec. 1973. Grant RF 1624

Current industrial practice and theory applicable to the fabrication of low-voltage p-channel metal-oxide-semiconductor (PMOS) devices is summarized. An extensive bibliography and design parameter graphs are presented.

11364

Cullen, G.W. and Corboy, J.F. (RCA Corp., David Sarnoff Res. Center, Princeton, NJ)
A COMPARISON OF THE SEMICONDUCTING PROPERTIES OF THIN FILMS OF SILICON ON SAPPHIRE AND SPINEL. J. of the Electrochem. Soc.: Solid-State Sci. and Technol. 121, no. 10, 1345-50, Oct. 1974

The Hall mobilities in 0.5 and 1.0μm thick heteroepitaxial silicon on (1102) sapphire and (100) and (111) spinel substrates are compared. The substrates employed were Czochralski sapphire, alumina rich flame fusion spinel, stoichiometric Czochralski spinel, and a "modified" alumina-rich Czochralski spinel. The semiconducting properties of the silicon on the spinels are similar if the Czochralski grown substrate surfaces are air annealed prior to deposition. The reproducibility achieved in electrical properties in silicon on spinel is related to the method of preparation of the substrate. In comparing the semiconducting properties in silicon on sapphire with silicon on spinel, one finds that the MOS transistor mobilities are more similar than the Hall mobilities.

11365

Goser, K. and Knauer, K. (Siemens AG, Res. Labs., Munich, Ger.)
NONVOLATILE CCD MEMORY WITH MNOS STORAGE CAPACITORS. IEEE J. of Solid-State Circuits SC-9, no. 3, 148-50, June 1974

The volatility of information stored in a charge-coupled device (CCD) can be avoided by storing the information in metal nitride-oxide silicon (MNOS) capacitors added to a CCD. In the following, the function, layout, and measured results of test circuits are described, and different layouts of such memory circuits are discussed.

11366

Rodgers, T.J. and Meindl, J.D. (Stanford U., Electronics Labs., Stanford, CA)
VMOS: HIGH-SPEED TTL COMPATIBLE MOS LOGIC. IEEE J. of Solid State Circuits SC-9, no. 5, Oct. 1974. 1974 International Solid State Circuits Conference

A new logic structure has been presented which takes advantage of v-groove technology and DMOS concepts to produce a transistor which is well suited for use in high-speed, high-density, 5V supply applicatons. VMOS logic in its present form is superior to gold-doped TTL in switching speed and power-speed product, and more dense than static NOR NMOS or I^2L for similar design rules. VMOS processing is a combination of well-known steps and the anisotropic etch. Important device parameters are will controlled by noncritical diffusion techniques.

11367

Tammaru, E. (Stanford U., Electronics Labs., Stanford, CA)
EFFICIENT TESTING OF COMBINATIONAL LOGIC CELLS IN LARGE-SCALE ARRAYS. Rept. no. SEL-68-040, Tech. Rept. no. 4601, 120 pp., May 1968. AD 836 051. Nonr-225(83). NR 373 369

This research investigates the characteristics that regular cellular arrays must have in order that each cell can be tested from the peripheral terminals of the array. The nominally identical cells in the array have n inputs and n outputs, where each of the n outputs is some combinational function of the n input variables of the cell. Of special interest is the characterization of cells and arrays in order to predict whether defective cells can be not only tested but also located within the array.

11368

Brotherton, S.D. and Singh, M.P. (U. of Southampton, Southampton, Gt. Britain)
INFLUENCE OF CLOCK WAVEFORMS ON THE PERFORMANCE OF CHARGE COUPLED DEVICES. Solid-State Electornics 17, no. 9, 981-84, Sept. 1974

A theoretical analysis of charge transfer in 3-phase C.C.D.'s has been performed for realistic clock pulses. The performance of the device with linear and exponential pulse edges is compared with the performance predicted by the conventional stepped pulse analysis, and it is shown that more efficient charge transfer is obtained with the latter driving technique.

11369

Gregory, B.L. and Gwyn, C.W. (Sandia Labs., Albuquerque, NM)
RADIATION EFFECTS ON SEMICONDUCTOR DEVICES. Proc. of the IEEE 62, no. 9, 1264-73, Sept. 1974

The radiation induced degradation of semiconductor material parameters is reviewed. These results are related to the degradation of semiconductor-device performance. Design techniques for minimizing the radiation-induced degradation are evaluated. Emphasis is placed on the effects of ionizing radiation on MOS structures. Transient ionization effects and circuit latchup are considered. The present degree of understanding of radiation effects in silicon devices is summarized.

11370

Manchester, K.E. (Sprague Elec. Co., Worcester, MA)
ION IMPLANTATION OFFERS FLEXIBILITY TO THE IC DESIGNER. Electronic Packaging and Production 15, no. 7, 5 pp., July 1975

Ion implantation is no longer a laboratory curiosity in the semiconductor field but has become a fully accepted production processing technique which can introduce well-described distributions of ions reproducibly and accurately at low temperature.

11371

Boxil, D.R. (RCA Corp. Govt. Commun. and Automated Systems Div., Burlington, MA)
PRODUCTION ENGINEERING MEASURES AUTOMATIC ASSEMBLY OF HYBRID INTEGRATED CIRCUITS. Rept. no. 16108, Quart. Prog. Rept. no. 3, Aug. 1-Oct. 31, 1974. ARPA Oid 386. DAAB05-73-C-2039

Effort has been initiated to develop automatic techniques and equipment capable of mass production of thick film hybrid integrated circuits. The amplifier trigger circuit, Army Part. no. 11715226, used in the XM734 multi-option fuse has been selected as the assembly which will serve as the test vehicle.

11372

Carnes, J.E., Kosonocky, W.F. and Levine, P.A. (RCA Labs., Princeton, NJ)
MEASUREMENTS OF NOISE IN CHARGE-COUPLED DEVICES. RCA Rev. 34, no. 4, 553-65, Dec. 1973. N00039-73-C-0014. 1972 International Electron Devices Meeting

Experimental data are presented that verify the present theory of noise fluctuations in the operation of charge-coupled devices. This includes the correlated transfer noise due to trapping of charge signal by fast interface states and white noise associated with optical and electrical introduction of input into a CCD register. Experimental results are also given on the operation of an input circuit to a CCD register for introduction of signal with noise fluctuations that are less than shot noise.

11373

Muehldorf, E.I. (IBM Corp., Systems Dev. Div., Manassas, VA)
A QUALITY MEASURE FOR LSI COMPONENTS. IEEE J. of Solid-State Circuits SC-9, no. 5, 291-97, Oct. 1974

Large-scale integration (LSI) components are subjected to testing based on stuck fault modeling. A stuck fault is a logic fault, where the terminal of a logic block assumes a fixed logic value and is said to be stuck. Stuck fault testing often does not provide patterns for all possible stuck conditions that can exist in a circuit. Because of the incompleteness of test coverage, a new quality measure is needed--one that is not based on sample inspection. Such an LSI quality measure is described in this paper.

11374

Beattie, J.A.C. (Royal Aircraft Establ., Gt. Britian)
MULTILAYER INTERCONNECTION TECHNIQUES FOR INTEGRATED CIRCUITS AND THEIR APPLICATION TO SPACECRAFT ELECTRONIC SYSTEMS. Rept. no. BR29572, Tech. Rept. 72090, 30 pp., June 1972. AD 906 425

Multilayer integrated circuits are described and results of recent work by Standard Telecommun. Labs. Ltd. outlined. The use of the technique for space electronics systems is compared with the hybrid assembly method developed at RAE and with conventional large scale integration (LSI). It is concluded that the multilayer technique is potentially more reliable than hybrid and cheaper than LSI.

11375

Kjar, R.A., Kinoshita, G., Butcher, D.T. et al. (No. Am. Rockwell, Res. and Technol. Div., Electronics Group, Anaheim, CA)
HARDENED MOST INPUT AND OUTPUT CIRCUITRY VOL. I. Rept. no. AFAL-TR-72-213, Rept. no. C71-587/501, Final Rept., May 12, 1971-Mar. 1, 1972, 74 pp. May 15, 1972. AD 902 280L. F33615-71-C-1586

This report describes an effort to extend previous work which demonstrated technology for fabricating radiation-resistance MOS Circuitry. The hardening approach employed in the program was based upon methods for growing the gate insulator--including chromium-doping of the oxide to reduce permanent ionizing-radiation damage in p-channel MOS structures--and upon silicon-on-sapphire (SOS) isolation to reduce transient radiation effects. This volume summarizes the unclassified results of the program which concerned (1) reliability evaluation of the previously developed radiation hardened 32-bit shift register, and (2) design and development of radiation-hardened MOS/SOS circuitry with emphasis on developing input/output circuitry to meet the interface requirements of a hardened system.

11376

Fisher, H.D. (Royal Aircraft Establ., Gt. Britain)
HYBRID MICROCIRCUIT TECHNOLOGY IN THE BRITISH NATIONAL SPACE PROGRAMME. Rept. no. BR34641, 34 pp., Dec. 1972. AD 913 950. 22nd Technical Symposium of the Avionics Panel of Advisory Group for Aerospace Research and Development. Rome, Italy, May 31-June 4, 1971

This paper describes an experimental equipment to be flown on the X3 Satellite in the British National Space Programme and develops arguments in support of the use of hybrid microcircuits for very high quality low volume production of electronic circuits. The current techniques are described in detail and reasons for the choice of technologies given. Process and component yields are given and future developments discussed.

11378

Weirick, L.J. (Sandia Labs., Met. and Electroplating Div., Livermore)
A METALLURGICAL ANALYSIS OF STRESS-CORROSION CRACKING OF KOVAR PACKAGE LEAD. Solid State Technol. 18, no. 3, 25-30, Mar. 1975. AT-(29-1)-789

Scanning electron microscopy and metallographic analysis indicated that stress-corrosion cracking was responsible for some Kovar leads completely breaking away from integrated circuit packages following a moisture-resistance test. The cracks were found to have been initiated intergranularly and propagated transgranularly. Further analysis showed that the following factors accelerated the stress-corrosion cracking: (1) the presence of a tensile stress (2) insufficient nickel plating on the Kovar, (3) penetration of the Kovar grain boundaries by copper and (4) the presence of contaminants containing free chloride.

11379

Richardson, W.S. (Motorola Semiconductor Prod., Phoenix, AZ)
DIAGNOSTIC TESTING OF MOS RANDOM ACCESS MEMORIES. Solid State Technol. 18, no. 3, 31-34, Mar. 1975

Diagnostic testing as performed by a design engineer is described as a necessary and valuable tool. Since diagnostic testing requires flexibility, the specific requirements for a memory test system and the hardware necessary to support the basic memory test system are discussed. An example of a memory disturb problem is explained in detail to illustrate the difficulty in identifying circuit sensitivities in an MOS random access memory.

11380

Anon.
APPLICATION OF NEW METHODS AND TECHNIQUES FOR FAILURE ANALYSIS. Solid State Technol. 18, no. 3, 38-40, Mar. 1975

This article presents a summary of papers on new methods and techniques for failure analysis presented at the 1974, 12th Annual Reliability Physics Symposium Problem areas are defined. The review papers on metallurgical failure modes are summarized. MOS drift mechanisms papers are also summarized.

11381

Bindell, J.B. (Bell Telephone Labs., Inc., Allentown, PA)
SCANNING ELECTRON MICROSCOPY AND RELATED ELECTRON BEAM TECHNIQUES IN IC TECHNOLOGY. Solid State Technol. 18, no. 4, 45-50, Apr. 1975

The Scanning Electron Microscope has become a very sophisticated instrument which has many uses in an electronics manufacturing environment. In this article, the uses of the SEM in this domain are reviewed and it is stressed that the SEM has many uses other than pure high resolution imaging.

11382

Casterline, E.T. (Microwave Semiconductors Inc., Somerset, NJ) and Benjamin, J.A. (Raytheon Co., Burlington, MA)
TRENDS IN MICROWAVE POWER TRANSISTORS. Solid State Technol. 18, no. 4, 51-56, Apr. 1975

The interplay between technology, design and reality in the construction of bipolar microwave transistors and their effects on the state-of-the-art, along with projections for future results are discussed in simple terms relating physical effects with processing constraints.

11383

Lucey, R.J. and Firman, A.H. (Teradyne, Inc., Boston, MA)
PROCESS MONITORING IN TRANSISTOR PRODUCTION. Solid State Technol. 18, no. 4, Apr. 1975

"Process monitoring" is a technique for keeping closer track of the final testing and manufacturing processes. This technique can greatly improve the efficiency of a production/test facility by reducing the amount of retesting that would otherwise be required as a result of faulty final testing, and by providing an insight into the production process and the long-term changes that occur in it.

11384

Agajanian, A.H. (IBM System Prod. Div., East Fishkill, NY)
A BIBLIOGRAPHY ON SEMICONDUCTOR DEVICE ISOLATION TECHNIQUES. Solid State Technol. 18, no. 4, 61-65, Apr. 1975

A literature search on semiconductor device isolation techniques was performed and a bibliography of 150 references was compiled. Electrical and Electronics Abstracts and Engineering Index of January 1965 to September 1974 were the main sources used in this search. Selected articles from the literature prior to 1965 are also included in this bibliography. For easy access to the needed references, the bibliography is divided into eighteen sections. A cross reference is given at the end of each section.

11385

Hakim, E.B. and Shappirio, J.R. (U.S. Army, ECOM, Electronic Technol. and Devices Lab., Fort Monmouth, NJ)
FAILURE MECHANISMS IN GOLD METALIZED SEALED JUNCTION DEVICES. Solid State Technol. 18, no. 4, 66-68, Apr. 1975

Two different types of p-n-p transistors and an integrated circuit, which were fabricated using silicon nitride and gold contact metallization, failed while on test in the Panama Canal Zone. Failure analysis indicated that the following failure mechanisms and problem areas were present in these units: (1) gold corrosion resulting in dendritic growth; (2) titanium over nitride between conductors; (3) exposed high concentrations of platinum; (4) inability of glass to adhere to gold metallization and to seal the device. These conditions occur as a result of both poor quality control and basic process limitations.

11386

Rottmann, H.R. (IBM System Prod. Div., East Fishkill, NY)
PHOTOLITHOGRAPHY IN INTEGRATED CIRCUIT MASK METROLOGY. Solid State Technol. 18, no. 6, 29-34, June 1975. Reprinted from IBM J. Res. and Dev. 18, no. 3, May 1974

Photoresist technology is shown to have important advantages over the use of high-resolution silver halide films in dimensional metrology for integrated circuit masks. Experimental techniques are shown for the use of photoresist and chrome images in the study of image quality and uniformity and in analysis of the causes of image degradation. This method is applied to "in situ" lens evaluation and to the measurement of the precision of photorepeater stepping tables used in mask fabrication. In addition, the value of 0.3 μm is established as the practical limit of dimensional tolerance in the present photolithographic technology, and its significance to the advancement of the state-of-the-art in mask manufacture is discussed.

11387

Danley, L.W. (Motorola Semiconductor Prod., Inc., HF Prod. Dev., Phoenix, AZ)
A METALLIZATION SYSTEM FOR MICROWAVE AND UHF POWER TRANSISTORS. Solid State Technol. 18, no. 6, 35-39, June 1975

Metal migration, a problem prevalent in aluminum-interconnected semiconductors operated at high current densities and elevated temperatures, has necessitated an industry search for production-grade metallization systems of higher reliability. Although the use of copper-aluminum, silicon-aluminum or other aluminum alloys, (plus rigorously controlled processing conditions), greatly reduces the risk of premature metal contact failure, the performance achieved is often just barely adequate. Various parameters of importance in a system that eliminates the problems associated with aluminum are discussed. Equipment procurement, process finalization and results (using SEM photomicrographs) are described.

11388

O'Malley, A.J. (GCA/David W. Mann, Burlington, MA)
TECHNOLOGICAL IMPLICATIONS IN THE PHOTOMASKING PROCESS. Solid State Technol. 18, no. 6, 40-45, June 1975

Growing demand for more sophisticated integrated circuit functions and performance challenges the designer to maximize the available chip area. Concurrently, the device manufacturer must produce at highest efficiency to maintain a profitable position in the marketplace. Maximum yield of finished IC's signals a successful return on capital equipment investment. Photomask making is reviewed here as it responds to demands of today's IC technology. Some critical areas of photomasking are examined within the frame of reference of the technological demands being placed on the operation, and how manufacturing equipment and techniques can meet present as well as anticipted requirements for maximum yield of highest density IC's.

11389

Lasky, D. (ILC Technol., Sunnyvale, CA)
EMULSION MASK PROCESSING TECHNIQUES. Solid State Technol. 18, no. 6, 46-50, June 1975

High resolution photographic plates account for approximately 75% of the production working masks in the semiconductor industry. The low cost of high resolution mask blanks apparently offsets their relatively poor yields and short mask lives compared to hard surface masks (chrome iron oxide, etc.). Methods of improving yield and lowering the costs associated with photomasking operations are constantly being explored. This article presents a state-of-the-art survey on emulsion mask processing and drying techniques, methods and equipment. Processing and drying are the largest single contributors to overall masking yields.

11390

Ronen, R.S. and Micheletti, F.B. (Rockwell Internatl., Electronics Res. Div., Anaheim, CA)
RECENT SOS TECHNOLOGY, ADVANCES AND APPLICATIONS. Solid State Technol. 18, no. 8, 39-46, Aug. 1975. Semicon/West '75. San Mateo, CA , May 22, 1975

Current SOS technology is described and several significant developments in the past five years are highlighted. Recent interest in SOS has been high both for conventional commercial applications and for many special requirements that cannot be filled by other technologies, particularly in military systems. Progress in the SOS area depends heavily on improvement in the material, rather than invention of novel circuit concept.

11391

Clark, K.G. (Canon-M.I.T. (U.K.) Ltd., Engl.)
AUTOMATIC OUT-OF-CONTACT MASK ALIGNMENT Solid State Technol. 18, no. 8, 8 pp., Aug. 1975

Mask alignment relies on the ability of an operator to position a photomask over a patterned wafer, and micropositioning control while viewing through a split field microscope. Equipment in current use makes contact between the photoresist surface and the photomask during exposure thus increasing the possibilities of damage to both photoresist film and the expensive target-carrying photomask. Considerable die yield improvement and greatly increased mask lifetime is achieved by manufacturers using out-of-contact wafer alignment techniques.

11392

Moritz, H. (IBM, Boelblingen, Ger.)
AUTOMATED METAL ETCH SYSTEM FOR IC-MANUFACTURE. Solid State Technol. 18, no. 8, 54-57, Aug. 1975

In integrated circuit manufacture, the subtractive etch process is widely used to provide the metal wiring lines. A uniform metal film is vacuum-evaporated and subsequently, unwanted metal is etched away. To account for various possible variations a considerable over-etch time is necessary. In effect this limits circuit density. An automated etch system is described, which etches one wafer at a time. Etch time is variable and controlled by an etch end-point detector. This results in optimized etching of each single wafer and high product yields.

11393

Matare, H.F. (Internatl. Solid State Electronics Consultants, Los Angeles, CA)
WAFER TESTING. Solid State Technol. 18, no. 8, 58-62, Aug. 1975

A survey of the principal methods available for wafer testing is presented. Diagnositc techniques are discussed which are used in connection with the identification of dopant profiles, materials composition, crystal perfection, oxygen content, vacancy clusters, swirls, striations and voids. Among the most important methods available are scattered light measurements, capacitance measurements, infrared microscopy, electroreflectance, spreading resistance, and photoelectric scanning. Photoelectric scanning has promise as a technique for rapid and nondestructive wafer testing.

11394

Kjar, R.A. and Kuhlmann, G.J. (Rockwell Internatl. Corp., Electronics Res. Div., Anaheim, CA)
RADIATION RESISTANT CMOS/SOS CIRCUITRY. Rept. no. C74-454/501, Final Rept., 59 pp., Apr. 1975. N00014-74-C-0416

This report describes the results of an investigation of CMOS/SOS circuits and processes for optimizing radiation hardness and reliability. Bias-temperature-stress and radiation tests were conducted on MOS transistors and CMOS inverter circuits fabricated using several different processing techniques. A versatile mask set of containing several variations of the basic 4007 triple-inverter circuit was designed for use in future process optimization studies and for fabricating demonstration devices.

11395

Gasparek, E.P. (GE, Heavy Military Equip. Dept., Syracuse, NY)
CHARGE COUPLED DEVICE SIGNAL PROCESSORS. Vol. I, Semiann. Rept., June 1, 1973-Jan. 1, 1974, 191 pp., Jan. 1974. AD/B-000 581L
Vol II, Final Rept., Jan. 1-Oct. 1, 1974, 125 pp., Oct. 1974. AD/B-000 582L. DAAB07-73-C-0336

Volume I documents effort to develop Charge Coupled Devices (CCD) Signal Processors for remote sensor applications. The effort was divided into two phases. First, a study was performed to define the characteristics of acoustic, magnetic, and seismic sensors. The results of this study effort were then used to define the performance characteristic desired for the CCD Signal Processor. The report gives a detailed discussion of the characteristics of the CCD devices and also compares theoretical versus actual output signals for various input waveforms. Volume II documents effort consisting of a study phase which updates the results of the study performed in Vol. I. Then a higher performance CCD correlator was designed and built during the remaining time.

11397

Senhouse, L.S., Jr., Kushler, D.L. and Murphy, B.T. (Bell Telephone Labs., Inc., Murray Hill, NJ)
BASE DIFFUSION ISOLATED TRANSISTORS FOR LOW POWER INTEGRATED CIRCUITS. IEEE Trans. on Electron Devices ED-18, no. 6, 355-58, June 1971

Base diffusion isolated transistors (BDI) designed for low power, nonsaturating, integrated circuits have been fabricated. Buried collectors are unnecessary in these low power devices, resulting in structures equivalent to discrete transistors in complexity purposes. Transistor characteristics differ negligibly from those of standard transistors at collector currents 0.05 mA, and are satisfactory for application in linear circuits at currents up to at least 0.1 mA. Transistor f_T is 80 MHz at 0.1 mA emitter current, 2 V collector voltage.

11398

Evans, W.J., Tretola, A.R., Payne, R.S. et al. (Bell Labs., Murray Hill, NJ)
OXIDE-ISOLATED MONOLITHIC TECHNOLOGY AND APPLICATIONS. IEEE J. of Solid-State Circuits SC-8, no. 5, 373-80, Oct. 1973

This paper described the use of selective oxidation and ion implantation to fabricate integrated circuits. The technique of selective oxidation is used to fabricate a "walled emitter" structure as proposed by Panousis. This allows a substantial reduction in transistor size, for a given active area, over standard fabrication techniques. The implantation provides some process simplification and results in excellent control over device parameters.

11399

McCaughan, D.V., Kushner, R.A. and Wagner, S. (Bell Labs., Murray Hill, NJ)
COMPLETE REMOVAL OF SODIUM FROM SILICON DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS. J. of the Electrochem. Soc.: Solid-State Sci. and Technol. 121, no. 5, 724-25, May 1974

Alkali ion contamination of thermally grown SiO_2 films on silicon is a serious problem in semiconductor technology. One technique which has been used with some success in alleviating this difficulty is the formation of a layer of phosphosilicate glass over either gate dielectric or passivating oxide. Phosphosilicate films are known to getter mobile ionic impurities. Here we present evidence that sodium initially present only near the SiO_2/Si interface in amounts comparable to those found in contaminated gate oxides ($\sim 10^{12}/cm^2$ Na) is removed to less than detection limits during phosphorous diffusions of short duration.

11400

McCaughan, D.V., Murphy, V.T. and Walden R.H. (Bell Telephone Labs., Murray Hill, NJ)
SOME PITFALLS IN FAST RAMP C-V MEASUREMENTS. Solid-State Electronics 16, no. 12, 1423-27, Dec. 1973

The triangular voltage sweep or fast ramp C-V method, while leading to an easy measurement of deep depletion C-V curves, may have pitfalls for the unwary, particularly in the case of degraded oxides. Two examples of the difficulties associated with the measurement in the presence of positive oxide charge, viz. (i) a distorted fast ramp C-V curve at intermediate bias values and; (ii) a "peak" in the curve due to an inversion layer surrounding the device, are illustrated and explained.

11401

Wagner, R.S., Sinha, A.K., Sheng, T.T. et al. (Bell Labs., Murray Hill, NJ)
TUNGSTEN METALLIZATION FOR LSI APPLICATIONS. J. of Vacuum Sci. & Technol. 11, no. 3, 582-90, May/June 1974

It is shown that MOS-LSI devices can be satisfactorily metallized with tungsten thin films using the rf-diode sputtering technique. The effect of sputtering power and of substrate bias was studied on the deposition rate, substrate temperature, and various properties of the film such as electrical resistivity stress, impurity concentration, constitution, and microstructure. The present process of W-film deposition has been found to offer several advantages. Low-power and low-voltage operation results in high quality MOS-compatible W-films. These factors make the present metallization process very suitable for CCD (single-level metallization) as well as LSI-IGFET (two-level metallization) applications.

11402

Gnadinger, A.P. and Rosenzweig, W. (Bell Labs., Allentown, PA)
POLARIZATION AND CHARGE MOTION IN METAL-Al_2O_3-SiO_2-Si STRUCTURES. J. of the Electrochem. Soc.: Solid-State Technol. 121, no. 5, 700-05, May 1974

An investigation of the flatband voltage shifts of double insulator MIS capacitors under bias temperature stress had been performed in order to assess and characterize the stability of double insulator IGFET's. These shifts were opposite to the applied bias voltage ("ionic" direction), and it was found that they are composed of two components: (a) A "Fast" component which is linear with gate bias voltage and symmetric with bias polarity. (b) A slow component which is observed under positive bias. It is characterized by a linear dependence of flatband voltage shift on the logarithm of stress time for times larger than a delay time, which is thermally activated.

11406

Rickers, H.C., Jr. and Walker, R.C. (IIT Research Inst., Reliability Analysis Center, RADC, Griffiss AFB, NY)
LSI TECHNOLOGY EVALUATION. Rept. no. RAC-75-14RM, 59 pp., Oct. 10, 1975

In addition to the modification of existing technologies, numerous technologies have been developed for the fabrication of LSI devices. Each of these technologies offers certain benefits and disadvantages which are related to the physical properties of the fabrication techniques. While the application requirements are often used as the criteria for the selection of a technology, the reliability characteristics should also be considered in this selection process. This report discusses the fabrication steps and physical properties of the major LSI technologies and the reliability aspects of these technologies.

11407

Chaffee, E.G. and McCammon, J.W. (Litton Ind., Electron Tube Div., San Carlos, CA)
DEVELOPMENT OF HIGH RELIABILITY RF KEYED CROSSED FIELD AMPLIFIER.
Rept. no. ECOM-73-0151-F, Final Rept., Apr. 15, 1973-May 15, 1975, 87 pp., July 1975. DAAB07-73-C-0151

This report describes the design, construction and testing of the L-5429-02 S/N 1 and S/N 2. The design was based on previous L-5429 design. Major modifications to the cooling circuit, rf matches, and new helix material and cathode support were incorporated to increase the power-handling capability of the device. Good operation was obtained from both tubes in a new permanent magnet package. These tubes were shipped to U.S. Army, ECOM, Fort Monmouth, NJ.

11408

Kern, W. (RCA Labs., Princeton, NJ)
DETECTION AND CHARACTERIZATION OF LOCALIZED DEFECTS IN DIELECTRIC FILMS. RCA Rev. 34, no. 4, 655-91, Dec. 1973

Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical dielectric films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and insulators of particular interest include thermally grown silicon dioxide and layers of vapor-deposited silicon dioxide, silicate glasses silicon nitride, aluminum oxide and complex silicates in thicknesses ranging from several hundred angstroms to several micrometers. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing dielectric breakdown, selective chemical etching, electrolytic decoration, liquid-crystal techniques, electron, probe microanalysis, and ion microprobe mass analysis.

11409

Pocock, D.N. (Northrop Corp., Hawthorne, CA)
COMPUTER-AIDED VULNERABILITY ANALYSIS OF A DIGITAL-TO-ANALOG CONVERTER.
Rept. no. AFWL-TR-74-140, Final Rept., July 26, 1973-May 21, 1974, 122 pp., Mar. 1975. F29601-73-C-0115

The goal of this program was to apply previously developed simplified microcircuit modeling techniques to the analysis of a real subsystem in order to identify problem areas and demonstrate the state-of-the-art. The subsystem studied is part of the flight instrumentation used in the E4A (military version of Boeing 747) aircraft. The overall problem approach was that of an engineering vulnerability analysis of the subsystem. The individual components were experimentally characterized and modeled, and the component models were then interconnected to obtain a simulation of the entire Digital/Analog converter using the MINI-SCEPTRE computer code. The computer simulation is used to predict both the transient and semi-permanent ionizing-radiation induced errors of the D/A converter, as well as the normal electrical characteristics. Comparison of computer predictions and experimental data demonstrates agreement to within the repeatability of component samples. The major problem is the long computer run time and associated cost for a single photoresponse prediction.

11411

Bushmire, D.W. and Chavez, E.L. (Sandia Labs., Albuquerque, NM)
DEVELOPMENT OF A COMPLAINT BONDING CAPABILITY FOR BEAM LEAD DEVICES. Rept. no. SLA 74-0217. 25 pp., July 1974

Compliant beam lead bonding is a method of thermocompression bonding that is relatively insensitive to variations in device beam hardness and thickness. It also permits the beams to be bonded with minimum bugging. An acceptable range of bonding parameters was developed by bonding and testing 200 devices. The optimized parameters were tool force (12-35 lbs.), and bond time (1 sec. to 5 sec.)

11412

Torrero, E.A.
FOCUS ON IC ANALOG SWITCHES AND MULTIPLEXERS. Electronic Design 23, no. 18, 64-72, Sept. 1, 1975

When high voltage complementary-MOS (CMOS) analog switches and miltiplexers first appeared several years ago, their performance far exceeded that of earlier p-channel and n-channel MOS (NMOS) versions. Suddenly, monolithic switching circuits could handle a wide range of analog input voltages without large changes in their ON resistances. Some of those early CMOS units were prone to latchups and occasionally even burnouts. Now imporved monolithic circuits have arrived, and they overcome the deficiencies of their predecessors. In fact, progress has showered us with several alternatives, not only in CMOS but in NMOS and junction FETs (JFETs) as well.

11413

Lehning, H. (Institu für Theoretische Electrotechnik, Technische Hochschule Aachen, West Ger.)
CURRENT HOGGING LOGIC (CHL)--A NEW BIPOLAR LOGIC FOR LSI. IEEE J. of Solid State Circuits SC-9, no. 5, 228-33, Oct. 1974. International Solid-State Circuits Conference. Philadelphia, PA Feb. 1974

Logic functions of current hogging logic are established by switching the lateral injection current in intermediate collector p-n-p structures. High functional density is achieved, since NOR, NAND, and complex gates can readily be realized and all logic elements can be placed within a common isolation region. CHL is fabricated with a standard buried collector process, and hence is compatible with linear bipolar circuits and other bipolar logic families. Current levels are employed as the logical variables, and the transfer characteristics of an AND-NOR gate are discussed. CHL offers high static and dynamic noise immunity. The paper demonstrates a static frequency divider as an example of an CHL circuit.

11414

Analog Devices Semiconductor, Norwood, MA)
BEWARE THOSE FET OP-AMP SPECS. Electronic Design 23, no. 1, 104-07, Jan. 4, 1975

Though this type of IC amplifier excels in low bias currents, self-heating and nulling effects can alter the other specs. Integrated circuit FET-input op amps have become the preferred choice in applications calling for very low input-bias currents. Bipolar amplifiers just can't compete with the picoampere and even sub-picoampere bias levels offered by the FET's. Data sheets abound with misleading and omitted specifications, making evaluation and selection a tough nut.

11415

Pao, H.C., Gunsager, K., Guadagna, J. et al. (Fairchild Camera and Instr. Corp., Fairchild Space and Def. Systems, Syossett, NY)
MEMORIES FOR RADAR. Rept. no. AD-AX-63, Interim Tech. Rept. 24 pp., May 11-Oct. 31, 1974. F33615-73-C-1044

The major efforts yet to be performed are the fabrication and test of the 16,384 line addressable random access memory devices, and testing of the 32,768 bit devices which are the final goal of the program. These efforts are scheduled for completion in May and June 1975. Technical information is given on the design and development of the 16 K and 32 K parts as well as a description of operating characteristics of the now completed 9K part (LA-9216).

11416

Dell'Oca, C.J., Kopp, R. and Sheehy, J. (Fairchild Camera & Instr. Corp., Fairchild Semiconductor, Mountain View, CA)
INVESTIGATION OF THIN-FILM SILICON PROCESS FOR RADIATION HARDENED MIS INTEGRATED CIRCUITS. Rept. no. AFCRL-TR-74-0378, Sci. Interim Rept. no. 1, 17 pp., July 1974. AD/B001 108L.
F19628-74-C-0109

Silicon thin films defined by electrochemical etching are being used as starting material in the simultaneous construction of junction-field-effect and metal-insulator-semiconductor devices. These devices will be fabricated in thin (1.0-2.μ0m) single-crystal films electrically isolated from a polysilicon supporting layer by thin dielectric films of both silicon dioxide and silicon nitride. Basic manufacturing techniques and modifications are described; elemental difficulties in determining the material properties of such thin semiconductor films are outlined. Process development and efforts to design an optimized photographic-mask set are reported. Finally, a brief description of the design and purpose of several test structures included in the forthcoming mask set is presented.

11417

Kamins, T.I. (Fairchild Camera and Instr. Corp., Res. and Dev. Lab., Palo Alto, CA)
DEFORMATION OCCURRING DURING THE DEPOSITION OF POLYCRYSTALLINE-SILICON FILMS. J. of the Electrochem. Soc. 121, no. 5, 681-84, May 1974

The deformation sometimes observed during the deposition of thick polycrystalline-silicon films for dielectrically isolated integrated circuits has been investigated. The degradation of films deposited by the decomposition of dichlorosilane, silane, or silicon tetrachloride in a hydrogen carrier gas has been observed to occur during the deposition rather than during the cooling cycle and to be more severe at lower deposition temperatures. This degradation has been related to the inclusion of trace quantities of gaseous contaminants, especially oxygen, in the structure of the film. The elimination of these contaminants from the deposition chamber allows the reproducible fabrication of high quality films.

11418

Robinson, A.T. and Bauer, L.O. (Hughes Res. Labs., Malibu, CA)
MANUFACTURING METHODS FOR ION IMPLANTATION. Interim Rept. no. 7, July 1-Sept. 30, 1971, 9 pp., Oct. 1971. AD 889 957L F33615-70-C-1238

This quarter marked the planned transfer of the Manufacturing Ion Implantation System from Malibu to Newport Beach. During the first portion of the quarter the System underwent extensive reliability testing. The test results indicated that with some modifications, the system reliability could be improved significantly. This rework involved principally the target chamber and the associated electronic monitoring and control equipment. The remainder of the quarter was spent in redesign and modifications of subsystems and existing hardware.

11419

Gates, H.P., Jr., Gourary, B.S., Deitchman, S.J. et al. (Inst. for Def. Analyses, Arlington, VA)
ELECTRONICS-X: A STUDY OF MILITARY ELECTRONICS WITH PARTICULAR REFERENCE TO COST AND RELIABILITY. VOL. I: EXECUTIVE CONSPECTUS. Rept. no. R-195, Final Rept., Feb.-Oct. 1973, 86 pp., Jan. 1974. AD 783 007. DAHC15-73-C-0200

This report identifies the current DOD and industrial policies, procedures, and practices in development, production, and operational support that most significantly influence the cost and reliability of military electronics, and it recommends changes to reduce and control cost and to improve reliability. The report concentrates on five major, high-impact areas: (1) data processing software, digital system architecture, design evolution, configuration management, project management, data costs, cost estimating, collection and feedback. (2) requirements, (3) competition and management options, (4) reliability enhancement and (5) maintenance training. Numerous other areas are discussed, and detailed recommendations are made in each.

11421

Shields, M. (Signetics, Bipolar Memory Div., Sunnyvale, CA)
SIGNETICS PROM RELIABILITY. 9 pp.

Fusible Link Technology has been intensively investigated at Signetics over the last six years with Field Programmable Read Only Memories (PROMs) being offered for sale since late 1971. This experience has enabled Signetics to produce a series of "second generation" TTL Schottky and ECL PROM circuit families, manufactured in a dedicated, high volume production area under strict process controls and to one basic process. Along with producbility, the emphasis on the product and process development programs involved in this new series has been:

- Reliability
- Programming Yield
- Device Performance

11423

Cotter, L.D. and Donaldson, M.A. (Intelcom Rad Tech., San Diego, CA)
USE OF INTEGRATED CIRCUITS IN FUTURE SATELLITES. Rept. no. AFWL-TR-74-94, Final Rept. Mar.-June 1973, 60 pp., Mar. 1975. AD/A003 021L. F39601-72-C-0124

This report surveys the status of radiation hardening of integrated circuits and their use in satellites. Included also in this report is a discussion of several semiconductor device classes and their generic radiation responses.

11424

O'Kane, D.F. and Mittal, K.L. (IBM Corp., Gen. Prod. Div., San Jose, CA)
PLASMA CLEANING OF METAL SURFACES. J. of Vacuum Sci. and Technol. 11, no. 3, 567-9, May/June 1974

Mild plasma cleaning of metal surfaces was shown to be effective in removing organic contaminants. Auger electron spectroscopy and surface wettability measurements were used to evaluate the plasma cleaning procedure and to provide a comparison with conventional solvent cleaning methods.

11425

Frieser, R.G. (IBM Systems Prod. Div., East Fishkill Facility, Hopewell Junction, NY)
CHARACTERIZATION OF THERMALLY GROWN SiO_2 SURFACES BY CONTACT ANGLE MEASUREMENTS. J. of Electrochem. Soc. no. 121, no. 5, 669-72, May 1974

This paper discusses recent advances in the study of solid surfaces by contact angle measurements which appeared promising in developing a technique to characterize different types of amorphous or polycrystalline metal and oxide surfaces. The extent to which contact angle measurements and spreading pressure values can be used to characterize various silica surfaces is explored. A practical scheme is offered using water and an organic solvent to characterize various silica surfaces in a simple and nondestructive manner.

11426

Shatzkes, M., Av-Ron, M. and Anderson, R.M. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY)
ON THE NATURE OF CONDUCTION AND SWITCHING IN SiO_2. J. of Appl. Phys. 45, no. 5, 2065-77, May 1974

Results are presented concerning high conduction and switching in Al-SiO_2-Si sandwich structures. The high conduction state is filamentary and is governed mainly by the voltage across the sandwich. It is relatively insensitive to variations in device geometry. Periodic current oscillations are observed for certain combinations of series load resistance and applied voltage. Once the high-conduction state is achieved, it can be maintained at applied voltages below the one required to cause the transition but larger than a minimum voltage, which may be related to the minimum ionization energy in SiO_2. Fluctuations are observed that depend on external circuit configuration, i.e., the load line, and on the ambient temperature. A physical model is presented in an attempt to provide a qualitative explanation of the origin of this form of characteristic. Local damage is evident whenever the high conduction state is seen (even with a single 50-nsec pulse). Electron microscopic analysis of a damaged region is presented.

11427

Osburn, C.M. and Bassous, E. (IBM, Thomas J. Watson Res. Center, Yorktown Heights, NY)
IMPROVED DIELECTRIC RELIABILITY OF SiO_2 FILMS WITH POLYCRYSTALLINE SILICON ELECTRODES. J. of the Electrochem. Soc. 122, no. 1, 89-92, Jan. 1975

Time dependent dielectric breakdown of SiO_2 films in MOS structures is shown to be strongly dependent on the electrode material used. Polycrystalline silicon electrodes give substantially longer times to failure than do aluminum electrodes. The improvement is 3-4 decades at 300°C; and, because of the larger activation energy for wearout with poly-Si (2.4 eV) compared to Al (1.4 eV), the relative advantage would be 8-16 decades at room temperature. Although time to breakdown is a strong function of SiO_2 thickness when the electrode is Al, it is nearly independent of thickness for structures having poly-Si electrodes.

11428

Baxter, G.K. and Brouillette, J.W. (GE, Electronics Lab., Syracuse, NY)
THERMAL RESISTANCE OF MICROELECTRONIC PACKAGES. Rept. no. R75ELS027, Tech. Info. Series, 70 pp., May 1975

This report summarizes the results of computer-aided analyses and of measurements performed in the laboratory during this contract. Infrared and electrical (temperature sensitive parameter) tests were performed on a series of thermal test packages containing a special thermal test chip; infrared tests were performed on commercial MIL-M-38510 packages containing the vendor's chip devices Infrared tests were also performed on two hybrid integrated circuit (HIC) packages and those results are included. Computer-aided simulations of the thermal test chip on various chip carriers (substrates) were performed to generate theoretical data for comparisons with the experimental test data. The comparisons and evaluation of test methods therefrom are discussed herein.

11429

Baxter, G.K. (GE, Electronics Lab., Syracuse, NY)
A NEW RECOMMENDED METHOD 1012 (THERMAL CHARACTERISTICS) FOR MIL-STD-883. Rept. no. R75ELS026, Tech. Info. Series, 30 pp., May 1975

This new method specifies test procedures, measurement locations and descriptive notations for measuring and specifying junction peak temperature, junction average temperature and junction region temperature, chip carrier temperature, relative thermal time constants and relative thermal resistance values for microelectronic packages. These methods will enable a user to make direct comparisons between thermal data provided by different vendors; and moreover, the data provide a meaningful interface for integrating vendor's data into the thermal design of the user's electronic system.

11430

Takahashi, M., Nishida, H., Kasai, T. et al. (Hitachi, Ltd., Kokubunji, Tokyo, Japan)
FABRICATION OF BUBBLE MEMORY CHIPS. IEEE Trans. on Magnetics MAG-10, no. 4, 1067-71, Dec. 1974

In this paper, described in detail is photolithography for fabrication of permalloy T-bar circuits with emphasis on achieving pattern accuracy and uniformity. This includes investigations of accurate imaging of mask patterns on photoresists and development of permalloy chemical etchants that cause little undercutting. Also discussed are step coverage and pattern defects.

11432

Gunsagar, K.C., Guidry, M.R. and Amelio, G.F. (Fairchild CCD Res. and Dev. Lab., Palo Alto, CA)
A CCD LINE ADDRESSABLE RANDOM-ACCESS MEMORY (LARAM). IEEE J. of Solid-State Circuits SC-10, no. 5, 268-73, Oct. 1975. F33615-73-C-1044

A novel approach to charge-coupled device (CCD) memory organization has been conceived and implemented in a 16 384-bit memory chip. It utilizes an isoplanar n-channel silicon gate MOS process in conjunction with self-aligned implanted barrier, buried channel CCD technology. The chip is organized in four parallel, identical sections of 32 independent lines with each line 128 bits long. The four sections are controlled in parallel. Any of the 32 lines (the same line in each of the four sections) can be randomly accessed; hence the name, line addressable random-access memory (LARAM). Each line can be brought to a halt at any of its 128 possible positions. Design features and test results of the memory are described.

11433

IEEE
13TH ANNUAL PROCEEDINGS, RELIABILITY PHYSICS 1975. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. Las Vegas, NV , 279 pp., Apr. 1-3, 1975. IEEE Cat. no. 75CH0931-6 PHY

Table of Contents

11434

Abbas, S.A. and Barile, C.A. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY)
P-CHANNEL REWRITABLE AVALANCHE INJECTION DEVICE (RAID) OPERATION AND DEGRADATION MECHANISMS. pp. 1-5. 13th Annual Proceedings, Reliability Physics 1975

To implement an electrically rewritable device for Read Mostly Memory applications, the structure of the FAMOS device is modified by incorporating an additional metal gate on top of the floating polysilicon gate and separated from it by a specially grown thermal oxide. Electrical erasure is accomplished by applying a positive voltage pulse to the metal gate. The "write" voltage has been lowered by using ion implantation. Reliability and charge retention are discussed and their impact on the design of the device is assessed. An empirical model for the conduction of oxide between the floating gate and the metal gate is developed and results are projected and compared with data obtained on the device.

11435

Dockerty, R.C. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY)
DEGRADATION MECHANISMS IN REWRITABLE N-CHANNEL FAMOS DEVICES. pp. 6-9. 13th Annual Proceedings, Reliability Physics 1975

Electrically rewritable n-channel FAMOS devices were fabricated with a floating polycrystalline silicon gate and an Al control gate. The Al gate is used to control injection of holes or electrons from the avalanching drain diffusion onto the floating gate. Charge retention by the floating gate and device degradation due to multiple write/erase cycling is discussed.

11436

Yang, D.Y., Johnson, W.C. and Lampert, M.A. (Princeton U., Dept. of Elec. Eng., Princeton, NJ)
A STUDY OF THE DIELECTRIC BREAKDOWN OF THERMALLY GROWN SiO_2 BY THE SELF-QUENCHING TECHNIQUE. pp. 10-14. F19628-72-C-0298. 13th Annual Proceedings, Reliability Physics 1975

The dielectric breakdown of SiO_2 films thermally grown on (100) silicon substrates was studied by the self-quenching technique, using thin aluminum field plates. The breakdown regions show distinct differences among the four possible combinations of substrate type and polarity of applied voltage. With p-type substrate and positive field-plate polarity, an anisotropy is observed which reflects the crystallographic structure of the substrate. A pre-breakdown instability, which is enhanced at lowered temperatures, is ascribed to hole-electron pair production in the oxide followed by hole trapping at or near the negative electrode.

11437

Grunthaner, F.J. and Maserjian, J. (JPL Calif. Inst. of Technol., Pasadena, CA)
SODIUM IONS AT DEFECT SITES AT SiO_2/Si INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY. pp. 15-25. 13th Annual Proceedings, Reliability Physics 1975

X-ray photoelectron spectroscopy (XPS) is described in its application as a probe for studying defects such as sodium in SiO_2 films. A general description is given of key experimental methods in XPS. New techniques are described for applying and monitoring a fixed bias at the surface of the oxide during the XPS measurement. In the deliberately Na-doped samples, five spectral peaks are distinctly observed and related to different defect states at the vacuum/SiO_2 and SiO_2/Al interfaces. An attempt is made to correlate the observations with previously reported models.

11438

Maserjian, J., Kaw, R. and Collier, J. (JPL, Calif. Inst. of Technol., Pasadena, CA)
TUNNEL INJECTION INTO GATE OXIDE TRAPS. pp. 26-33. 13th Annual Proceedings, Reliability Physics 1975

An experimental method is described for measuring the density of oxide traps in the gate oxide of an MOS transistor as a function of energy and position near the silicon interface. Measurements are obtained from different oxide growth processes and after Co^{60} irradiation. The results are related to long-term drift of threshold voltage.

11439

Lee, S.N. and Kjar, R.A. (Rockwell Internatl. Corp., Anaheim, CA)
SOS ISLAND EDGE PROFILES FOLLOWING OXIDATION. pp. 34-37. 13th Annual Proceedings, Reliability Physics 1975

A study of silicon and oxide profiles at the edges of silicon islands etched in silicon-on-sapphire (SOS) has shown that, following thermal oxidation of the silicon, a "V"-shaped groove forms between the silicon dioxide grown on the island edge and the sapphire substrate. This groove can cause etching and metal coverage anomalies at the island edges resulting in poor circuit yield and reliability.

11440

Libove, C. (Syracuse U., Syracuse, NY)
RECTANGULAR FLAT-PACK LIDS UNDER EXTERNAL PRESSURE: FORMULAS FOR SCREENING AND DESIGN. pp. 38-47. 13th Annual Proceedings, Reliability Physics 1975

Formulas are presented for the maximum tensile stresses in the lid seal and the maximum lid deflections of a rectangular flat-pack under external pressure. These formulas can facilitate (a) the proper design of the package so that it will retain its hermeticity under a given screening pressure and (b) the selection of a proper pressure to use in the hermeticity screening of an already designed package. Information is also given on the approximate equivalence of external pressure and centrifuge acceleration in regard to the seal stresses and lid deflections of a rectangular flat-pack.

11441

Meyer, D.E. (Tex. Instr., Dallas, TX)
MINIATURE MOISTURE SENSORS FOR IN-PACKAGE USE BY THE MICROELECTRONICS INDUSTRY. pp. 48-52. F30602-74-C-0203. 13th Annual Proceedings, Reliability Physics 1975

This work entails developing an in-package moisture sensor which was begun not because the technique of mass spectrometry was lacking, but because analysis by mass spectrometry is costly, time consuming and destructive. As a result even though it has been proven that moisture does significantly contribute to failure, we do not yet know what are unacceptable levels of moisture in a package. It is the purpose of this communication to report on work accomplished, draw attention to difficulties and technical problems, give specific examples of how sensors have been used, and to suggest what the future may hold for small and sensitive moisture sensors in the microelectronics industry.

11442

Hanley, L.D. and Martin, J.H. (Charles Stark Draper Labs., Inc., Cambridge, MA)
A TEST OF PARYLENE AS A PROTECTIVE SYSTEM FOR MICROCIRCUITRY. pp. 53-57. F04701-74-C-0343. 13th Annual Proceedings, Reliability Physics 1975

The principal objective of the test program reported in this paper was to determine whether it is at all reasonable to use parylene as a protective system for microcircuits in place of a hermetic seal in high reliability equipment. A radiation-hardened circuit containing nichrome resistors was selected as a test specimen because of its considerable sensitivity to humidity failure The circuits were operated in a ring-counter configuration during humidity tests. Non-parylened units both with and without lids were also tested as controls, and other parylene-coated units were kept in a dessicator.

11443

Fitch, W.T. (Motorola Inc., SPD, Phoenix, AZ)
THE DEGRADATION OF BONDING WIRES AND SEALING GLASSES WITH EXTENDED THERMAL CYCLING. pp. 58-69. F30602-72-C-0251. 13th Annual Proceedings, Reliability Physics 1975

This program was undertaken to study the degradation of wire bond strength in ceramic and metal flat packages and dual in-line packages when subjected to 1020 Method 1010C (-65/+150°C) temperature cycles or 1020 Method 1011C (-65/+150°C) thermal shock cycles. The second part studies the degradation of ceramic dual in-line package seal strength when subjected to 1005 Method 1011A (0-100°C) thermal shock cycles.

11444

Jellison, J.L. (Sandia Labs., Albuquerque, NM)
SUSCEPTIBILITY OF MICROWELDS IN HYBRID MICROCIRCUITS TO CORROSION DEGRADATION. pp. 70-79. 13th Annual Proceedings, Reliability Physics 1975

The study included three areas of investigation. First, characterization of broken aluminum-silver microwelds which lead to the tentative conclusion that the bond degradation could be due to corrosion. Next,extensive environmental tests were conducted which confirmed that aluminum-silver bonds are highly susceptible to corrosion. Finally, the analysis of silver-frit capacitor termination surfaces identified contaminates that accelerated corrosion of aluminum-silver bonds. In addition to the principal study of aluminum-silver bonds, additional environmental tests were conducted to evaluate the susceptibility of other dissimilar metal bond pairs to corrosion.

11446

Shumka, A. and Piety, R.R. (JPL, Calif. Inst. of Technol., Pasadena, CA)
MIGRATED-GOLD RESISTIVE SHORTS IN MICROCIRCUITS. pp. 93-98. 13th Annual Proceedings, Reliability Physics 1975

The investigations on the migrated-gold resistive shorts (MGRS) in microcircuits using a multilayer TiW-Au-TiW metallization system are reported here. The purpose of the paper is to describe the characteristics of this new failure mode, identify the failure mechanisms, present a failure model for the MGRS and identify the most probable cause of the problem. Finally, three possible techniques for screening potential MGRS problems will be presented.

11447

Grunthaner, F.J., Griswold, T.W. and Glendening, P.J. (JPL, Calif. Inst. of Technol., Pasadena, CA)
MIGRATORY GOLD RESISTIVE SHORTS: CHEMICAL ASPECTS OF A FAILURE MECHANISM. pp. 99-105. 13th Annual Proceedings, Reliability Physics 1975

In this paper, we propose a model for MGRS failure mode. The chemistry of the system will be reviewed. More detailed considerations of dendritic growth from electrochemical and electrostatic perspectives will be given. Results of experiments directed to model these concepts will be presented. These will be followed by a discussion of the application of these results and concepts to the present case. Particular emphasis will be placed on the question of a threshold water concentration for MGRS failure. Finally, several possible corrective actions will be suggested.

11448

Agarwala, B.N. (IBM, Poughkeepsie, NY)
ELECTROMIGRATION FAILURE IN AU THIN-FILM CONDUCTORS. pp. 107-12. 13th Annual Proceedings, Reliability Physics 1975

The present study is aimed at identifying the dominant atom transport mode and determining the primary damage mechanism in Au films. Studies are carried out to determine the dependence of lifetime on current density, stripe temperature, degree of surface coverage, and type of coating element. The possible sources of atom flux divergences are ascertained from direct observations of the damage.

11449

Macpherson, A.C., Weisenberger, W.H., Day, H.M. et al. (U.S. Navy, Nav. Res. Lab., Washington, D.C.)
EFFECTS OF FAST TEMPERATURE CYCLING ON ALUMINUM AND GOLD METAL SYSTEMS. pp. 113-20. 13th Annual Proceedings, Reliability Physics 1975

Microwave power transistors used in radar systems are pulsed at kilo-cycle rates during operation and typically undergo from 10^8 to 10^{12} cycles during lifetime. The power dissipated in these devices is sufficient to cause a large temperature swing during each pulse. In this paper emphasis is placed on metal failures which result from temperature cycling as distinguished from such effects as electromigration or metal-to-metal, metal-to-oxide and metal-to-silicon chemical interactions which arise from long time high temperatures and which show up on conventional accelerated life tests.

11450

Berger, R.G. and Gregoritsch, A.J. (IBM, Essex Junction, VT)
INDUCED PASSIVATION DEFECT STUDY. pp. 121-27. 13th Annual Proceedings, Reliability Physics 1975

An n-channel FET memory array chip whose quartz passivation layer is purposely disrupted in specific nonrandom locations is used to study the propensity of these induced defects to fail due to localized inversion of the silicon surface stemming from positive ions contained within the defect which are residual from processing. Two distinct sizes of induced defects are considered; three and seven micron diameters; 800 of the larger size and 100 of the smaller. Data obtained from these temperature/voltage accelerated stresses is presented which shows time-to-fail is related to the ionic (mostly sodium) levels contained within the defects. It is also concluded that the experimental failures are of a classical inversion related nature.

11451

Bart, J.J. (U.S. Air Force, RADC, Reliability Phys. Sect., Griffiss AFB, NY)
ANALYSIS OF DEPOSITED GLASS LAYER DEFECTS. pp. 128-35. 13th Annual Proceedings, Reliability Physics 1975

The intent of the paper is to review the types of defects which limit the chemical protection properties of glass layers. The studies were performed on single layer metallized bipolar and CMOS devices submitted for failure analysis or physical characterization at RADC, Griffiss AFB. The remainder of this paper will describe the nature and source of the glass layer defects. The inter-relation of such factors as package type, glass deposition method, interconnect metallization layer type and device stress conditions will be examined. The reliability hazards associated with these defects will be discussed along with suggested improvements in device specification and testing.

11452

Mohsen, A.M., Retajczyk, T.F., Jr. and Haszko, S.E. (Bell Labs., Murray Hill, NJ)
FAILURE MECHANISM OF METAL-POLYSILICON-DOPED SILICON BUTTING CONTACTS. pp. 136-41. 13th Annual Proceedings, Reliability Physics 1975

The metal-polysilicon-doped silicon butting contact is presently widely used in MOS silicon gate integrated circuits because it occupies minimum area on the chip and does not require additional photolithography. A possible failure mechanism of this contact with self-aligned, ion-implanted sources and drains has been observed. Recent data obtained on processes used to fabricate two-phase, two-level polysilicon CCDs are presented. Results show that oxide etching under the edges of the polysilicon gate during contact window definition can lead to excessive leakage due to metal-to-substrate shorts at the metal-polysilicon-doped silicon butting contact.

11453

Scoggan, G.A. and Peressini, P.P. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY) and Agarwala, B.N. (IBM System Prod. Div., Poughkeepsie, NY) and Brouillard, A. (IBM World Trade Corp., Corbeil Essonnes, Fr.)
WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN Al-Cu, Al-Cu-Si, AND Ag CONDUCTORS. pp. 151-58. 13th Annual Proceedings, Reliability Physics 1975

Electromigration-induced failures observed in thin-film conductors can strongly influence device reliability. With the current demand for higher packing densities in integrated circuits, the effect of width on stripe reliability has become a subject of some importance. Previous studies have shown that the life-time of Al conductors decreases when stripe width is reduced. However, no data are available on the variation of lognormal standard deviation σ with stripe width. The objective of the present work was to determine the dependence of the median lifetime t_{50} and of σ on the conductor width.

11454

Philbrick, J.W. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY) and DiStefano, T.H. (IBM T.J. Watson Res. Center, Yorktown Heights, NY)
SCANNED SURFACE PHOTOVOLTAGE DETECTION OF DEFECTS IN SILICON WAFERS. pp. 159-67. F19628-74-C-0077. 13th Annual Proceedings, Reliability Physics 1975

A scanned surface photovoltage (SSP) method is capable of detecting a wide variety of defects in a silicon surface. This method can be used to scan a large area of the silicon surface, which is coupled by a surface channel to a small remote electrode. The resolution obtained, about 2μm, is explained theoretically in this paper for the case of a differentiated photovoltage signal and a small (0.8 μm diameter) light beam from an optimized optical system. SSP images of a variety of defects, both naturally occurring and induced, were obtained along with images produced by other methods for comparison.

11455

Donnelly, T.M. and Powell, W.W. (Hughes Aircraft Co., Culver City, CA) and Dobson, J. (U.S. Air Force, RADC, Solid State Appl. Sect., Griffiss AFB, NY) and Devaney, J. (Hi-Rel Labs., San Marino, CA)
EFFECTS OF PROGRAMMING VARIATIONS ON NICHROME LINK PROMS. pp. 168-73. F30602-74-C-0156. 13th Annual Proceedings, Reliability Physics 1975

Devices from two separate PROM manufacturers utilizing nichrome technology were subjected to variations in programming pulses to determine effects on the fusible links. After programming, devices were chemically etched and a Scanning Electron Microscope (SEM) analysis was donducted on the selectively programmed fuses. A rectahgular pulse corresponding to the vendors programming specification was used to program the fuses. However, during programming the pulse amplitude was adjusted to simulate the effect of variations in energy levels delivered by the on-chip addressing circuitry to the fusible links. The amplitudes were adjusted to extend the time required for fusing to a range of 100 s to several seconds. Under SEM examination, the appearance of the fused time during programming. A description of experiments performed, along with SEM photographs are presented.

11456

Ebel, G.H. (Singer Corp., Wayne, NJ)
TUTORIAL SESSION ON HYBRID TECHNOLOGY-INTRODUCTION. pp. 221-23. 13th Annual Proceedings, Reliability Physics 1975

Analysis shows that hybrids have a potential reliability improvement of 7 to 1 over discrete parts. Because of the complex nature of hybrid technology, the increased reliability can only be achieved by using proper controls. Although this is true for most components, the multi-discipline technology used to fabricate today's hybrids make the control problem both more difficult and necessary. The multitude of processes available to hybrid makers tends to result in new problems and some unique "fixes" to these problems. Some examples of these problems are discussed.

11457

Redemske, R.F. (Teledyne Microelectronics, Los Angeles, CA)
MULTILEVEL SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT ATTACH FOR HYBRID FABRICATION. pp. 224-29. 13th Annual Proceedings, Reliability Physics 1975

The interest in multilevel substrate technology arises from the fact that hybrid complexity and hybrid packaging density has been increasing for a number of years. As time goes on, integrated circuit dice have more and more connection pads as the industry moves toward MSI and LSI silicon technology. The result is that there is no practical way in a single layer structure of approaching the dice with the substrate stripes to obtain reasonable length wire bonds from the die pads to the substrate. This discussion relates to epoxy component attach for hybrids. Metal attach systems for large ceramic capacitors, under the impetus of thermal cycling and thermal shock, has produced microcracks in either a glazed substrate structure or in the ceramic of the capacitors itself. Analysis indicated this to be due to the fact that the temperature coefficient of expansion of the ceramic in the capacitor is different from that of the aluminum oxide substrate. It was found that the use of epoxy offered a practical solution. Epoxies display plastic deformation sufficient to accomodate the temperature coefficient difference and prevent the strains involved from becoming stresses.

11458

Lane, C.H. (U.S. Air Force, RADC, Griffiss AFB, NY)
PACKAGES AND FILM RESISTORS FOR HYBRID MICROCIRCUITS. pp. 230-41. 13th Annual Proceedings, Reliability Physics 1975

A review of resistor systems, and the processes used to deposit and delineate them, is given. Effects of mechanical, thermal, chemical and electrical stresses are discussed as they relate to accuracy and stability. Failure mechanisms are reviewed. Trimming techniques are explored and design limits for the various systems discussed. Parameters of interest such as frequency response, temperature coefficient, voltage coefficient and noise are compared for the various systems. Finally, quality control and screening techniques are discussed as they relate failure mechanisms and package quality and reliability control.

11459

Bertin, A.P. and Terwilliger, T.W. (GE, Aircraft Equip. Div., Utica, NY)
REPAIRS TO COMPLEX HYBRID CIRCUITS - THEIR EFFECT ON RELIABILITY. pp. 242-47. 13th Annual Proceedings, Reliability Physics 1975

Repairs properly made to hybrid circuits are dependable and do not cause a reduction in the overall reliability of the hybrid circuit. Repairing of technically complex hybrid circuits is a cost effective method and must be allowed to meet the systems cost effectiveness requirements of today's military systems. Repairs of hybrid circuits can be made both during processing, before seal while in the final package, and after seal. It is necessary to have specific repair rules, visual criteria, and overall controls in place to evaluate the repair. Constant monitoring of the screening results and repair processes is mandatory.

11460

Murphy, C. (Rockwell Internatl., Downey, CA)
HYBRID TECHNOLOGY LOOSE PARTICLES AND COATING MATERIALS. pp. 248-52. 13th Annual Proceedings, Reliability Physics 1975

Any discussion concerning particles in hybrids usually comes soon to the question of whether or not particles are really a problem. Conversation with a wide spectrum of hybrid users has led to the conclusion that problems associated with particles are a function of the sensitivity each user perceives to exist for his particulur application and program requirements. It is interesting to note, however, that almost all users state that even limited tests indicate that a percentage of all hybrids seems to exhibit the presence of particles. Previous studies of particle behavior clearly indicate that if particles occur, they can easily become mobile within the enclosure of microelectronic packages. The question that each hybrid user must answer for his particular application and environments is, "Am I really concerned that there will be particles in some of my hybrids?" If the answer is "no" the designer may happily concern himself with other quality aspects of his system; if the answer is "yes", the designer finds himself in the growing ranks of persons trying to do something about particles.

11461

Peck, D.S. (Bell Telephone Labs., Inc., Allentown, PA)
PRACTICAL APPLICATIONS OF ACCELERATED TESTING-INTRODUCTION. pp. 253-54. 13th Annual Proceedings, Reliability Physics 1975

The purpose of this tutorial session is to review some of the practical applications of accelerated testing, or testing at accelerated stress levels, with which at least some organizations have had experience in recent times. Those who still have doubts regarding the efficacy or the safety of these test conditions might benefit from hearing the experience of some of those who are using them, and it is the purpose of this session to hear some of these experiences and to provide a medium for discussing their applicability to other people's problems.

11462

Brodeur, J.E. (Fairchild Semiconductor, Mountain View, CA)
PROCESS CONTROL BY MEANS OF ACCELERATED TESTING. pp. 255-56. 13th Annual Proceedings, Reliability Physics 1975

High temperature operating life test gives quick feedback on the processes used in fabrication of semiconductor wafers. The relatively high failure rate of the (so-called) freaks is quickly demonstrated in such a test and can indicate a marginal or out of control process. This method of process control concentrates on the initial fallout as a means of determining the reliability of final products. Greater than 150°C stress temperatures should not be applied to plastic encapsulated devices. Since most epoxies have glass transition temperatures in the range of 150°C to 180°C permanent damage to the package could result.

11463

Lycoudes, N. (Motorola Semiconductor Div., Bipolar I/C Reliability Eng., Phoenix, AZ)
PRACTICAL USES OF ACCELERATED TESTING AT MOTOROLA. pp. 257-59. 13th Annual Proceedings, Reliability Physics 1975

The value of accelerated tests lies in their ability to create in a short period of time the same failure modes that would take much longer to occur under normal use conditions. At Motorola, accelerated testing is used extensively for evaluation of new products, process and material changes, long-term failure rate prediction and reliability line audits. This workshop presentation will examine three such tests: Temperature Humidity Bias; Pressure Temperature Humidity Bias; High Temperature Operating Life Test, and how they are used to provide timely solutions to everyday problems.

11464

Stitch, M. (McDonnell Douglas Astronautics Co., East, St. Louis, MO)
HIGH TEMPERATURE OPERATING TESTS (HTOT). A CONTROL FOR CONTAMINATED MICROCIRCUIT PROCESSES. pp. 260-62. 13th Annual Proceedings, Reliability Physics 1975

This paper addresses the application of HTOT burn-in as a microcircuit user's end-process test for process cleanliness. If the "freak" population can be economically eliminated, then we can obtain reliable, long life microcircuits. HTOT (200°C to 300°C) burn-in offers a viable, cost effective, method for controlling the number of contaminated device escapees. HTOT burn-in with the associated time-temperature-voltage relationships accelerates the demise of the "freak" population parts, while only using a negligible portion of the "main" population available life.

11465

VanVonno, N.W. (Harris Semiconductor, Melbourne, FL)
DETERMINATION OF USEFUL LIFE OF TWO-LAYER METALLIZATION SYSTEMS VIA ACCELERATED STRESSING. pp. 263-65. 13th Annual Proceedings, Reliability Physics 1975

Accelerated testing was utilized as a means of rapidly determining the reliability, under usage conditions, of a two-level aluminum metallization - SiO_2 structure with level-to-level via contacts. During step-stressing, two-level metallization test vehicles passivated with deposited SiO_2 layer showed greater immunity from electromigration than unpassivated structures. Further, the 0.25-mil via contacts failed sooner during constant accelerated stress testing than the 0.50-mil via contacts. The data presented here deal specifically with the outcome of accelerated testing of passivated and unpassivated via contacts. Based on these test results from 0.25-mil and 0.50-mil via contacts, the 0.50-mil via contact (fully passivated) was adopted as a design rule.

11466

Altman, L.
SPECIAL REPORT: C-MOS ENLARGES ITS TERRITORY. Electronics 48, no. 10, 77-88, May 15, 1975

Improved standard circuits have strengthened C-MOS's grip on process-control applications; greater chip complexity is opening up new jobs in communications, instruments, and computers.

11467

Chauhan, A.S. and Maheshwari, L.K. (Birla Inst. of Technol. & Sci. Dept. of Elec. & Electronics Eng. Pilani, Rajasthan, India)
X-RAY RADIATION EFFECTS ON SEMICONDUCTOR DEVICES. Indian J. of Pure & Appl. Phys. 13, no. 4, 226-28, Apr. 1975

The results of an experimental study of X-ray radiations on semiconductor devices, including junction diodes, transistors, and integrated circuits, are presented. It is shown that the storage time (t_s) in passivated diodes increases in the presence of radiations. The collector to emitter saturation voltage $V_{CE(sat)}$, initially increases and then becomes constant. The output drive current capability of integrated circuit logic gates is decreased in the presence of the radiations. It is suggested that the channel formation which takes place in device behaviour.

11468

Hewlett, F.W., Jr. (Bell Labs, Allentown, PA)
SCHOTTKY I^2L. IEEE J. of Solid-State Circuits SC-10, no. 5, 343-48, Oct. 1975

Schottky I^2L uses the principles of integrated injection logic (I^2L/MTL) and the properties of ion implantation to obtain improved performance at the same densities as conventional I^2L. Schottky diodes are formed in the multicollectors of the switching transistor and reduce the signal swing, thus improving the power delay efficiency. An increase in the intrinsic speed limit is also feasible. The Schottky I^2L structure and characteristics are described and contrasted with conventional I^2L. A model which is useful for its design is discussed. Integrated test structures which provide direct comparison between conventional and Schottky I^2L performance have been fabricated. The experimental results demonstrate a factor of 2 improvement in power delay efficiency of Schottky I^2L over conventional I^2L.

11469

Rosenbaum, S.D. and Caves, J.T. (Bell-Northern Res., Ottawa, Ontario, Can.)
8192-BIT BLOCK ADDRESSABLE CCD MEMORY. IEEE J. of Solid-State Circuits SC-10, no. 5, 273-80, Oct. 1975

Design data and experimental characteristics are given on an 8192-bit n-channel charge coupled memory device, intended for applications requiring shorter latency than ordinary MOS shift registers or fixed-head disks and at potentially lower cost than either MOS shift registers or random-access memories. This was achieved by dividing the array into 32 memory blocks of 256 bits each, with addressable, random access to any block, permitting average latency of approximately 100 μs. A two level overlapping polysilicon gate process was used, with conservative design tolerances. Power dissipation on-chip plus capacitive drive power during data access at 1 MHz is approximately 250 mW, and less than 5 mW during standby at 20 kHz with data retention.

11470

Nicholas, K.H., Ford, R.A. and Daniel, P.J. (Mullard Res. Labs., Redhill, Surrey, Engl.)
REDUCED GAIN OF ION-IMPLANTED TRANSISTORS. Appl. Phys. Letters 26, no. 6, 320-22, Mar. 15, 1975

Ion implantation is increasingly being used as a deposition technique because of the good uniformity and reproducibility that can be obtained with it. In this letter it is reported that lower gains of bipolar transistors can result from this use of implantation rather than diffusion for depositions. The degradation of gain is shown to be a lifetime effect associated with crystal damage. A technique for avoiding the degradation is described.

11471

Steiff, L.H.
L5 PHYSICAL DESIGN PUTS IT ALL TOGETHER. Bell Labs. Record 51, no. 10, 324-31, Nov. 1973

From the largest equipment bay to the controlled quantity of solder that positions the smallest chip component on an amplifier substrate, physical design transforms the L5 electrical design into an operating system. The result -- a tough, durable, reliable system.

11472

Boyle, G.R. and Pederson, D.O. (U. of Calif., Dept. of Elec. Eng. and Computer Sci., Electronics Res. Lab., Berkeley, CA) and Cohn, B.M. (Intel Corp., Santa Clara, CA) and Solomon, J.E. (Natl. Semiconductor Corp., Santa Clara, CA)
MACROMODELING OF INTEGRATED CIRCUIT OPERATIONAL AMPLIFIER. IEEE J. of Solid-State Circuits SC-9, no. 6, 353-64, Dec. 1974. F44620-71-C-0087. NSF Grant GK-17931. 1974 International Solid-State Circuits Conference. Philadelphia, PA, Feb. 1974

A macromodel has been developed for integrated circuit (IC) op amps which provides an excellent pin-for-pin representation. The macromodel is a factor of more than six times less complex than the original circuit, and provides simulated circuit responses that have run times which are an order of magnitude faster and less costly in comparison to modeling the op amp at the electronic device level. In addition, the performance of the macromodel in linear and non-linear systems is presented. For comparison, the simulated circuit performance when modeling at the device level is also demonstrated.

11473

Wen, D.D. (Fairchild Res. and Dev. Lab., Palo Alto, CA)
DESIGN AND OPERATION OF A FLOATING GATE AMPLIFIER. IEEE J. of Solid-State Circuits SC-9, no. 6, 410-14, Dec. 1974. N00014-72-C-0344

A unique amplifier configuration is examined that fully exploits the intrinsically high signal-to-noise performance of charge-coupled devices (CCD's). In this amplifier, the signal charge is detected with a conducting "floating gate" embedded in the oxide between a bias electrode and the silicon substrate. The change of voltage on the floating gate produced by the signal charge in the CCD channel is then used to modulate the current flow in a metal-oxide-semiconductor (MOS) transistor. The signal charge remains isolated and can be moved downstream in the CCD channel; thus, it can be detected again by other similar structures. Computer analysis, test structure design, and experimental results of a floating gate amplifier (FGA) are presented.

11475

Sutherland, P.G., Ahlport, B.T. and DeMartino, V. (Northrop Corp., Electronics Div., Palos Verdes Peninsula, CA)
BOND IMPROVEMENT PROGRAM FOR HARRY DIAMOND LABORATORIES. Rept. no. NORT 73-309A, Rept. no. HDL-TR-127-1, Final Tech. Rept., AD 782 886. DAAG39-73-C-0127

The major effort in this contract established process controls, monitoring techniques and production screening techniques for BLH die attach and beam bond processes. Discrete resistor substrate materials and epoxies for component mounting were evaluated for BLH processing compatibility and radiation hardening. Component mounting techniques were improved to obtain repeatable, void free component attachment for LSI devices. Nickel beam bond strength is established as 3 to 5 times greater than conventional flying wire. Repeatable results are achieved with the use of process controls such as bond monitoring, bond schedule optimization material parameter control, thermal-mechanical screening and 100% nondestructive beam bond pull testing.

11476

Johnson, G.M. (McDonnell Douglas Corp. McDonnell Douglas Astronautics Co. - East, St. Louis, MO)
EVALUATION OF HIGH TEMPERATURE (743°K - 573°K) ACCELERATED LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING METHODS. Rept. no. MDC-E1208, Final Rept., July 1973-Dec. 1974, 71 pp., Jan. 24, 1975. NAS5-22233

The application of high temperature accelerated test techniques was shown to be an effective method of microcircuit defect screening. Comprehensive microcircuit evaluations and a series of high temperature (473°K to 573°K) life tests demonstrated that a freak or early failure population of surface contaminated devices could be completely screened in thirty two hours of test at ambient temperatures above 473°K. Equivalent screening at 398°K, as prescribed by current Military and NASA specifications, would have required in excess of 1500 hours of test. All testing was accomplished with a Texas Instruments' 54L10, low power triple-3 input NAND gate manufactured with a Titanium Tungsten (TI-W, Gold (Au) metallization system.

11477

Card, H.C. (U. of Manchester Inst. of Sci. and Technol., Manchester, Engl.)
FACTORS AFFECTING AVALANCHE INJECTION INTO INSULATING LAYERS FROM A SEMICONDUCTOR SURFACE. Solid-State Electronics 17, no. 5, 501-2, May 1974

It is possible to produce an electron avalanche in the space-charge region formed at the surface of a semiconductor by a perpendicular electric field. In particular, a silicon surface region can be biased into avalanche breakdown by the application of a large a.c. signal provided the doping concentration is $\leq 10^{18}$ cm^{-3}. Hot carriers from the avalanche plasma normal to the surface can then be injected into the conduction or valence bands of an adjacent SiO_2 layer, giving rise to unidirectional currents and trapping.

11478

Berenbaum, L. (IBM)
COATING NARROW RESISTIVE LINES TO INCREASE ELECTROMIGRATION RESISTANCE. IBM Tech. Disclosure Bull. 17, no. 11, Apr. 1975

A typical cross section of an in-process wafer, wherein a well-known photoresist lift-off technique is utilized to produce thin resistive lines or stripes which are coated with suitable coating materials, is shown, such as CR, Ti and Ni, to reduce electromigration. With the lift-off process, a photoresist layer is spun onto a wafer, exposed by an electron beam, and developed so that shallow trenches exist. The conductive material is then deposited in the trenches, a coating material is applied and the photoresist is subsequently removed to expose the coated stripes.

11479

Schick, J.D. (IBM)
ELECTRICAL CONTACT THROUGH AN SiO_2 OVERLAY BY ULTRASONIC PROBE. IBM Tech. Disclosure Bull. 17, no. 11, Apr. 1975

Failure analysis of semiconductors having SiO_2 overlays cannot be completely performed, without electrical probing of aluminum lines under the overlay. This technique allows such probing and also aluminum line isolation.

11480

Anolick, E.S. (IBM)
AUTOMATIC DIELECTRIC QUALITY EVALUATING SYSTEM. IBM Tech. Disclosure Bull. 17, no. 10, Mar. 1975

An automatic dielectric quality evaluating system is shown. Kerf devices, such as simple capacitors for thick oxides or gate chains for field-effect transistor products, are incorporated into product wafers. The wafers are then brought singly to a probe station and heated to 200 to 250°C. The probe station could handle 50 capacitors simultaneously to save time per wafer.

11481

Ti, L.B. and Shang, D.C.T. (IBM)
ENVIRONMENTAL FILTER. IBM Tech. Disclosure Bull. 17, no. 9, Feb. 1975

Environmental filter uses electrostatic and chemical neutralization techniques to remove contaminants and pollutants from the air flow system associated with a semiconductor wafer processing line.

11482

Ho, I.T. Ku, S.M., Maley, G.A. et al. (IBM)
PROGRAMMABLE MEMORY CIRCUITS. IBM Tech. Disclosure Bull. 17, no. 11, Apr. 1975

Circuits are described utilizing integrated circuit resistors having values tailored by ion implantation. Each resistors is formed to have a specific value. Then, by ion implantation, the value of the resistor is raised, by as much as 20%. The use of increased current through the resistor sequentially returns it to its original value, thereby, enabling programming.

11483

Hsieh, C.M. (IBM)
CONTACT HOLE OPENING FOR FABRICATING A SCHOTTKY BARRIER DIODE. IBM Tech. Disclosure Bull. 17, no. 11, Apr. 1975

This process eliminates a severe metal discontinuity problem which exists at the contact hole step of a Schottky barrier diode.

11484

Blech, I.A. (Technion-Israel Inst. of Technol., Haifa, Israel) and Rosenberg, R. (IBM Systems Prod. Div., East Fishkill, Hopewell Junction, NY)
ON THE DIRECTION OF ELECTROMIGRATION IN GOLD THIN FILMS. J. of Appl. Phys. 46, no. 2, 579-83, Feb. 1975

The motion of gold atoms during electromigration in thin films is shown to be in the direction of the electron flow i.e. from cathode to anode. This is contrary to other observations reported in the literature in which holes are seen in the anode regions. In the present work, holes at the anode were produced by transient annealing effects of non-equilibrium grain structures and not by reversal of the direction of the electromigration. Holes can be regularly produced in either anode or cathode regions depending upon test conditions, preannealing, and heat sinking.

11485

Kasprzak, L.A. (IBM System Prod. Div. East Fishkill Facility, Hopewell Junction, NY)
HIGH RESOLUTION SYSTEM FOR PHOTORESPONSE MAPPING OF SEMICONDUCTOR DEVICES. Rev. Sci.Instrum. 46, no. 3, 257-62, Mar. 1975

A system has been built which employs a cw 6328 Å laser beam to excite the photoresponse of a semiconductor device. The excitation is achieved by focusing the laser beam to a 1μ spot on the surface of the device under investigation. Heretofore 5-10 resolution has been reported in the literature. Further, the optical path of the system is such that the device surface and spot are simultaneously in focus. A Pockel's cell is used to amplitude modulate the laser beam intensity. The result is a photoresponse at the characteristic amplitude modulation frequency of the Pockel's cell. A lock in amplifier, with a reference input at the characteristic amplitude modulation frequency, is used to amplify the photoresponse to the desired level. The result is a versatile, high-resolution system for the study of light-sensitive devices and phenomena. Programmed area scans have given qualitative and quantitative information about semiconductor diode and transistor junction properties near the semiconductor surface.

11486

Breed, D.J. (Philips Res. Lab., Eindhoven, Neth.)
NON-IONIC ROOM TEMPERATURE INSTABILITIES IN MOS DEVICES. Solid-State Electronics 17, no. 12, 1229-43, Dec. 1974

Recently it has been pointed out that considerable instabilities can occur in MOS devices under negative voltage bias at room temperature. These instabilities are observed by applying at room temperature a voltage to the gate of an MOS device, cooling under this voltage bias to 77°K and subsequently measuring the CV curve or the threshold voltage with the applied voltage bias. The instabilities are due to the generation of positive charges in the oxide and cause negative voltage shifts. In this paper the charging is described in terms of a thermally assisted tunnelling process. A model is presented for the observed time and temperature dependencies of the charging and associated activation energies.

11487

Declerck, G., Van Overstraetan, R. and Broux, G. (Katholieke U. Leuven, Dept. Elektrotechniek, Lab. Fysica en Elektronica, Belgium, Neth.)
MEASUREMENT OF LOW DENSITIES OF SURFACE STATES AT THE Si-SiO_2-INTERFACE. Solid-State Electronics 16, no. 12, 1451-60, Dec. 1973.

By a careful process Si-SiO_2-interfaces can be made with a low oxide charge Q_{ox} and with a low surface states density N_{ss}. For dry oxides on (100) N_{ss} - values as low as a few 10^9 cm^{-2} eV^{-1} are found on samples with an oxide charge density of 3.0×10^{10} cm^{-2}. Only the Nicollian-Goetzberger conductance method is proved to give reasonable results on these structures. The quasi-static low frequency C-V technique is in good agreement with the conductance technique for samples with N_{ss} - values higher than 1.0×10^{10} cm^{-2} eV^{-1}. The spatial fluctuation of surface potential, mainly caused by oxide charge fluctuations, is an important parameter when studying the high or low frequency C-V-characteristics. Some irregularities in the experimental N_{ss}-ψ_s-curves are explained.

11488

Taketa, Y. and Haradome, M. (Nihon U., Phys. Sci. Lab., Narashino, Japan)
THICK FILM RESISTORS WITH IMPROVED VOLTAGE STABILITY. IEEE Trans. on Parts, Hybrids, and Packaging PHP-10, no. 1, 74-81, Mar. 1974

Thick film resistors have been prepared by adding glass frits to the conductive materials of the resistors. By this method, it is found that the resistance of the glass phases in the thick film resistors decreases, with a resulting decrease of voltage drift after applying high voltage pulses to the resistors. In addition, the electrical properties and stability of these resistors are improved over resistors made from some present commercially available pastes.

11489

Arai, E. and Terunuma, Y. (Nippon Telegraph and Telephone Public Corp., Tokyo, Japan)
WATER ABSORPTION IN CHEMICALLY VAPOR-DEPOSITED BOROSILICATE GLASS FILMS. J. of the Electrochem. Soc.: Solid-State Sci. and Technol. 121, no. 5, 676-81, May 1974

Infrared absorption measurements have been made of physically adsorbed water and silanol in borosilicate glass films which were chemically vapor-deposited at 400°C and then exposed at room temperature to moist air of relative humidity 50±10%. Both the physically adsorbed water and silanol were found to increase with time up to about 10^5 min and then to decrease. The process of water adsorption sites of CVD glass were suggested to decrease with the increase of time.

11490

Benz, H.F. and Husson, C. (NASA, Langley Res. Center, Hampton, VA)
CHARGE COUPLED DEVICE (CCD) ANALOG SIGNAL PROCESSING. Proceedings of the IEEE 63, no. 5, 822-23, May 1975

Analog charge-coupled devices and sampled data filtering have developed into mature disciplines. Each discipline offers the other wide systems advantages where alone it would be impractical. This letter explores these advantages in a number of implementations against the scale of wide low-cost applications.

11491

Stoller, A.I. and Schlip, W.H. Jr, (RCA Labs. Princeton, NJ)
ISOLATION TECHNIQUES FOR FABRICATING INTEGRATED CIRCUITS. II. DIELECTRIC REFILL TECHNIQUES AND DECAL AIR ISOLATION. RCA Rev. 29, no. 4, 485-506, Dec. 1968

Three techniques are described for preparing silicon-integrated circuits in which the individual components are separated from one another by a true dielectric rather than the p-n junctions that are presently used. Two of these techniques begin with wafers in which devices have already been formed, while the third involves a new type of isolating substrate capable of undergoing diffusion steps. In all cases the devices are precisely located with respect to one another and are essentially coplanar, so that interconnections can be formed in a single operation.

11492

Vanstone, G.F., Roberts, J.B.G. and Long, A.E. (Royal Radar Establ., Worcestershire Engl.)
THE MEASUREMENT OF THE CHARGE RESIDUAL FOR CCD TRANSFER USING IMPLUSE AND FREQUENCY RESPONSES. Solid-State Electronics 17, no. 9, 889-95, Sept. 1975

By developing a model for the impulse response of a single phase CCD a simple equation is derived which relates the ratio of the first two pulses of the impulse response to the charge residual. When this is extended to practical multiphase structures it is shown that this equation is independent of the number of clock phases used in a CCD. Using Z transforms an expression for the frequency response of a CCD is derived in terms of charge residual. Values for the charge residual are obtained by experimental measurement of impulse and frequency responses and these are compared to test the validity of the model used.

11493

Guditz, E.A. and Burke, R.L. (MIT, Lincoln Lab., Lexington, MA)
MULTICHIP INTEGRATED CIRCUIT MEMORY WITH PHOTOFORMED PLATED CONDUCTORS. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 2, 89-96, June 1975

A 20 chip integrated circuit memory has been constructed utilizing techniques of plastic embedment, photoformation of plastics, and selective electroless metal deposition previously reported. It has been demonstrated that groups of passivated integrated circuit chips can be accurately placed in array positions, embedded in plastic, and interconnected with electroless nickel conductors deposited in photoformed multilayered conductor paths separated by selectively photoformed plastic dielectric layers. Thermal paths of nickel, plated directly to the backs of the chips and to an adhered photoetched metal substrate, effectively remove heat from the chips. The three laboratory phototypes, constructed to demonstrate this packaging technique, were operated under dynamic cyclic mode test conditions.

11494

Hampel, D. and Stewart, R.G. (RCA, Advanced Commun. Lab., Somerville, NJ)
EMP HARDENED CMOS CIRCUITS. Rept. no. HDL-TR-192-1, Final Rept., May-Oct. 1973, 35 pp., Oct. 1973. AD/A004 034. DAAG39-73-C-0136

A survey and testing program has shown that standard CMOS circuits will not survive EMP induced surges of more than 200 volts from a 50-ohm source. However, an analysis of the failure mechanism showed that bulk CMOS integrated circuits could be readily modified to survive EMP surges of up to 5,000 volts from a 50-ohm source. This new monolithic protection circuit is compatible with existing CMOS processing, and represents an extension of existing networks for static discharge protection.

11495

Boyle, W.S. and Smith, G.E.
CHARGE COUPLED SEMICONDUCTOR DEVICES. Bell Systems Tech. J. 49, no. 4, 587-93, Apr. 1970

This paper describes a new semiconductor device concept. Basically, it consists of storing charge in potential wells created at the surface of a semiconductor and moving the charge (representing information) over the surface by moving the potential minima. Schemes for creating, transferring, and detecting the presence or absence of the charge are discussed. In particular, we consider minority carrier charge storage at the $Si-SiO_2$ interface of a MOS capacitor. This charge may be transferred to a closely adjacent capacitor on the same substrate by appropriate manipulation of electrode potentials. Examples of possible applications are: a shift register, an imaging device, a display device, and a logic device.

11496

Williams R.A. (Rockwell Internatl. Corp., Electronics Res. Div., Anaheim, CA)
INVESTIGATION OF SOS PROCESSES FOR FABRICATION OF RADIATION HARDENED MIS DEVICES AND ICs. Rept. no. AFCRL-TR-74-0553, Rept. no. C74-830/501, Sci. Rept. no. 1, May 1-Oct. 31, 1974, 30 pp., Oct. 1974. AD/B002 838. F19628-74-C-0199

In this report investigation of the radiation hardening of MIS devices on SOS material was covered. Work has been directed toward understanding radiation-induced leakage mechanisms and experiments were designed to investigate the effects of radiation-induced trapped charge in the sapphire. Suitable devices were fabricated on SOS material using existing masks for a test structure designated MOS-X. Both n-type and p-type starting material covering a range of doping concentration was used, giving both enhancement and deep depletion mode transistors of both n-and p-channel types.

11497

Gehweiler, W.F. (RCA, Advanced Technol. Lab., Camden, NJ)
LOW POWER, HIGH SPEED CMOS/SOS CIRCUITS. Rept. no. ECOM-74-0508-F, Rept. no. ATL-CR-75-05, Final Rept., May 30-Nov. 30, 1974, 52 pp., Feb. 1975. AD/B002 640L. DAAB07-74-C-0508

The objective of this program was to determine the feasibility of using the low voltage CMOS/SOS technology to implement a low power waveform generator. The program consisted of the design and analysis of a direct digital frequency synthesizer and a test phase associated with characterizing the performance of similar but previously designed and processed test vehicles.

11498

Apfel, R.J. (Fairchild Semiconductor, Mountain View, CA) and Gray, P.R. (U. of Calif., Dept. of Elec. and Eng. and Comput. Sci., Berkeley, CA)
A FAST SETTLING MONOLITHIC OPERATIONAL AMPLIFIER USING DOUBLET COMPRESSION TECHNIQUES. IEEE J. of Solid-State Circuits SC-9, no. 6, 332-40, Dec. 1974

A new high-speed monolithic operational amplifier is described which uses an improved feedforward circuit configuration to achieve a total acquisition time (slewing plus settling) of 650 ns with a 10-V input step without compromising dc performance or requiring costly nonstandard processing.

11499

Amelio, G.F., Tompsett, M.F. and Smith, G.E.
EXPERIMENTAL VERIFICATION OF THE CHARGE COUPLED DEVICE CONCEPT. Bell System Techn. J. 49, no. 4, 593-600, Apr. 1970

Structures have been fabricated consisting of closely spaced MOS capacitors on an n-type silicon substrate. By forming a depletion region under one of the electrodes, minority carriers (holes) may be stored in the resulting potential well. This charge may then be transferred to an adjacent electrode by proper manipulation of electrode potentials. To test the assumption that this transfer will take place in reasonable times with a small fractional loss of charge, devices were fabricated and measurements made. Charge transfer efficiencies greater than 98 percent for transfer times less than 100 nsec were observed.

11500

Graf, A.J. and Doremus, L.W. (U.S. Army, Feltman Res. Lab., Picatinny Arsenal, Dover, NJ)
STUDY OF APPROACHES FOR IMPROVING PRODUCT RELIABILITY THROUGH RELIABILITY PHYSICS TECHNIQUES. Rept. no. PATM 2037, 34 pp., Apr. 1973. AD 910 829L

IIT Research Institute has been under contract with Rome Air Development Center for several years developing, implementing and now operating the RAC for DOD. The RAC is an important repository of data and experience which is available to assist the engineer interested in microelectronic reliability. On many components and devices RAC generates information during all phases of fabrication, testing and operation which is then collected, catalogued, analyzed and disseminated to government and contractor organizations through publications and direct inquiry.

11507

Boleky, E.J., Schlesier, K.M., Ipri, A.C. et al. (RCA Labs., Princeton, NJ)
ADVANCED CMOS CIRCUIT TECHNIQUES.
Rept. no. AFAL-TR-71-217 Final Rept., Apr. 1, 1970-Mar. 31, 1971, 74 pp., Aug. 1971
Rept. no. AFAL-TR-72-1, Rept. no. PRRL-71-CR-40, Final Rept., May 1-Oct. 30, 1971, 57 pp., Jan. 1972.
F33615-69-C-1499

Very high-speed MOS integrated circuits fabricated using silicon-on-sapphire (SOS) technology is described. A 256-bit dynamic CMOS/SOS Si-gate shift register was fabricated containing 2072 transistors in a 97 x 121 mil area, including bonding pads. It includes a recirculating feedback loop for serial memory use. A maximum shift register clock rate of 300 MHz using 15-V clock signals was predicted. Dynamic testing showed maximum operating clock frequencies in excess of 200 MHz at 10 V and stage capacitance values around 0.14 pF. Minimum operating frequencies were on the order of 20 kHz. A study is given of the compatibility of the SOS technology with two Al_2O_3 fabrication processes: plasma anodization and pyrohydrolytic (PHL) deposition. Emphasis was placed on the study of oxide compatibility with SOS technology and reducing its charge. Silicon films on sapphire that may be used in the fabrication of very-high-speed digital circuits of complex design are also described.

11508

Anon.
1975 INTEGRATED CIRCUIT APPLICATIONS CONFERENCE. Sponsored by the Electronic Engineering Times. Washington, D.C., Apr. 29, 30, May 6, 7, 1975. Boston, Mass. Apr. 30, May 1, 7, 8, 1975. Chicago, Ill., May 1, 2, 8, 9, 1975

Table of Contents:

11509

Goerner, R. (Teledyne Semiconductor, Mountain View, CA)
USING BIPOLAR LOGIC TO IMPROVE PERFORMANCE IN CMOS AND MICROPROCESSOR SYSTEMS. 1975 Integrated Circuit Applications Conference

The applications discussed in this paper reflect the speed, power and noise immunity advantages offered from various combinations of technologies in optimizing system performance. Many of the examples illustrate users' inputs regarding specific problems and solutions.

11510

Uimari, D. and Cavlan, N. (Signetics, Sunnyvale, CA)
FIELD PROGRAMMABLE LOGIC ARRAY. pp. 37-47. 1975 Integrated Circuit Applications Conference

This article discusses the advantages of Field Programmable Logic Arrays and how they differ from standard PROM's. Nichrome Fuse Technology and logic structure are also discussed.

11511

Miles, G. and Rice, R. (Fairchild Semiconductor, Mountain View, CA)
BIPOLAR MEMORY COMES OF AGE. pp. 69-98. 1975 Integrated Circuit Applications Conference

A number of major technical advances have been made in recent years in the field of semiconductor memories, particularly in the area of bipolar field of semiconductor memories, particularly in the area of bipolar devices. Fairchild Semiconductor has lead the way in with the introduction of the Isoplanar process in 1971, the first production bipolar 1024 random access memory (RAM) devices in 1972, production 1024 ECL RAMs in 1973, and low cost, low power and higher speed bipolar 1024 RAMs in 1974. The result is the unprecedented opportunity to implement simple design, large scale, super-performance memories at large volume production costs less than 1¢/bit, with further cost reductions available in the near future. Memory systems designers should re-analyze their choice of bipolar v.s. MOS memory components for many applications.

11512

Grebene, A.B. (Exar Integrated Systems, Inc., Sunnyvale, CA)
THE XR-2211- A PRECISION PLL SYSTEM FOR DATA COMMUNICATIONS. pp. 99-106. 1975 Integrated Circuit Applications Conference

The phase locked loop (PLL) is a versatile system block suitable for a wide range of applications in data communication systems, particularly in the areas of tone detection or FSK decoding. This application note describes the performance features and the applications of a third-generation monolithic PLL system which is specifically intended to overcome: 1) Temperature stability: The temperature drift of center frequency in the earlier monolithic PLL designs were of the order of 150 ppm/°C to 500 ppm/°C. 2) Frequency accuracy: For a given external setting, the center frequency of existing PLL's is only accurate to about ±10% of nominal design value, thus requiring additional potentiometers for fine tuning.

11513

Vander Kooi, M.K. (Siliconix Inc., Santa Clara, CA)
APPLICATIONS OF A 10Ω HIGH SPEED ANALOG SWITCH. pp. 107-12. 1975 Integrated Circuit Applications Conference

The new DG180, DG183, DG186 and DG189 analog switches offer a new horizon in very low ON resistance high speed I.C. analog switching. They offer a typical ON resistance of 7Ω with a guaranteed maximum of 10Ω at 25°C and over all signal ranges specified. The logic inputs are fully TTL, CMOS, DTL and RTL compatible. OFF and ON transition times are 250ns and 300 ns respectively (which gives a break-before-make operation between switches in a package) and OFF isolation is almost 60dB at 1 MHz.

11514

Nevala, B. and Pelletier, A. (Fairchild Semiconductor, Mountain View, CA)
BIPOLAR ECL/TTL RAM TESTING (A SIMPLE PLIGHT). pp. 141-58. 1975 Integrated Circuit Applications Conference

Testing strategies and the characteristics of available test equipment play a very important role in the production of high performance ECL and TTL Bipolar RAMs. Today's high performance Bipolar RAMs are all static designs and are extremely well behaved devices. Their sensitivites to pattern, supply voltages and temperature are low, and their requirements are straight-forward and simple. This well behaved and straightforward nature provides a great advantage to the user in the design, implementation and maintenance of memory systems. The high speed performance intrinsic to these devices, however, poses a different set of problems to test engineering personnel. The AC resolution, AC accuracy and general pulse and timing fidelity of even recently available memory test equipment are marginal. Improvements in these areas are slow in coming from production equipment manufacturers. In most cases, even the most advanced equipment needs to be further engineered and modified to approach the desired accuracy and resolution in timing measurements.

11515

Sevastopoulos, N. (Natl. Semiconductor Corp., Santa Clara, CA)
LF156: A NEW MONOLITHIC HIGH PERFORMANCE FET INPUT OP. AMPLIFIER. pp. 228-43. 1975 Integrated Circuit Applications Conference

Monolithic FET and bipolar input operational amplifiers both possess unique characteristics of which the design engineer should be aware. This paper compares the two technologies highlighting the advantages of the FET input system. Several applications of FET-input OP AMP IC's are illustrated.

11516

Kelley, S. (Motorola Semiconductor Prod., Phoenix, AZ)
APPLICATIONS OF DUAL RAMP A/D CONVERTERS. pp. 244-59. 1975 Integrated Circuit Applications Conference

Together the MC1505 and MC14435 form a dual slope, low speed, high bit resolution A/D converter. As such, it is a central building block of analog to digital measuring instruments. The MC1505 is a linear bipolar integrated circuit. The MC14435 is a CMOS digital part. The emphasis in their design was not toward putting an entire instrument on two chips, but toward providing two chips which perform the central and most difficult A to D operation with the accuracy and stability required in an industrial instrumentation market. Together they make temperature stable, accurate instrumentation possible in any A to D instrument. The two chip system includes a 3 1/2 digit accurate voltage reference and a system clock which any A to D must have. It does not include autopolarity, autoranging, or front end buffering, because these features should be designed to fit the measurement application for which they are intended. Thus, the versatility of the MC1505-MC14435 system is not limited by the specifications of its special features.

11517

Wittlinger, H.A. (RCA Solid State Div., Somerville, NJ)
UNDERSTANDING AND USING THE UNIQUE COS/MOS OP-AMP, RCA CA3130. pp. 260-64. 1975 Integrated Circuit Applications Conference

The introduction of the CA3130 COS/MOS Op-Amp marks another milestone in the continuing evolution of the ideal monolithic IC Op-Amp. Its characteristics in unique design features are reviewed in order to convey an appreciation of the universality with which it can be employed in circuit applications.

11518

1975 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE. DIGEST OF TECHNICAL PAPERS. Sponsored by the IEEE Solid-State Circuits Council, the IEEE Philadelphia Section and the University of Pennsylvania. Marriott Motor Hotel, Philadelphia, Penn., 244 pp., Feb. 12-14, 1975

Sessions:

Large Scale Integration
Optoelectronics
A/D and D/A Techniques
Frontiers of Technology
Microwave FETs
Computer Aids for IC Design and Testing
Microwave Oscillators and Amplifiers
High Speed Logic
Active Microwave Diode Circuits
Sampled-Date Analog Signal Processing
Advances in Solid- State Logic
Medical and Consumer Electronics
Analog Circuit Techniques

11520

Brammer, W.G., Erickson, J.J. and Levy, M.E. (Hughes Aircraft Co., Culver City, CA)
ELECTROMAGNETIC RADIATION SCREENING OF MICROCIRCUITS FOR LONG LIFE APPLICATIONS. Rept. no. NASA-CR-120512, Rept. no. P74-438, HAC Ref. no. DO573, Interim Rept., Nov. 1, 1973-Oct. 31, 1974, 125 pp., Oct. 1974. N75-10311. NAS8-30373

A theoretical and experimental study has been carried out on the utility of X-rays as a stimulus for screening high reliability semiconductor microcircuits. The theory of the interaction of X-rays with semiconductor materials and devices was considered. Experimental measurements of photovoltages, photocurrents, and effects on specified parameters were made on discrete devices and on microcircuits. The test specimens included discrete devices with certain types of identified flaws and symptoms of flaws, and microcircuits exhibiting deviant electrical behavior. With a necessarily limited sample of test specimens, no useful correlation could be found between the X-ray induced electrical response and the known or suspected presence of flaws.

11521

Finnila, R.M., Toombs, T.N. and Dill, H.G. (Hughes Aircraft Co.)
CMOS III: A HIGH DENSITY ION IMPLANTED CMOS TECHNOLOGY. 11 pp.

Modern high performance electronic systems often tax the capabilities of presently available technologies. Integrated circuits with very high speed or very low power consumption are required for many of these systems. Bipolar devices are still the choice for most high speed circuits, although silicon on sapphire MOS circuits may eventually replace them. CMOS circuits are already replacing bipolar circuits in power limited systems.

11522

Kamath, B.Y., Meyer, R.G. and Gray, P.R. (U. of Calif., Computer Sci. and Elec. Res. Lab., Berkeley, CA)
RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND SETTLING TIME OF OPERATIONAL AMPLIFIERS. IEEE J. of Solid-State Circuits SC-9, no. 6, 347-52, Dec. 1974

The effects of pole-zero pairs (doublets) on the frequency response and settling time of operational amplifiers are explored using analytical techniques and computer simulation. It is shown that doublets which produce only minor changes in circuit frequency response can produce major changes in settling time. The importance of doublet spacing and frequency are examined. It is shown that settling time always improves as doublet spacing is reduced whereas the effect of doublet frequency is different for 0.1 and 0.01 percent error bands. Finally it is shown that simple analytical formulas can be used to estimate the influence of frequency doublets on amplifier settling time.

11523

Davis, P.C. and Moyer, S.F. (Bell Labs., Reading,PA) and Sarri, V.R. (Bell Labs., Holmdel, NJ)
HIGH SLEW RATE MONOLITHIC OPERATIONAL AMPLIFIER USING COMPATIBLE COMPLEMENTARY P-N-P's. IEEE J. of Solid-State Circuits SC-9, 340-47, Dec. 1974

An internally compensated monolithic operational amplifier, fabricated using only junction-isolated bipolar processing, slews in excess of 500 V/μs, and settles to within 0.1 percent in 200 ns as a pulse inverter. Performance in the noninverting mode is only slightly degraded in comparison with the inverting mode. In addition, the following performance levels have been achieved: 50-MHz unity-gain bandwidth with 96-dB open-loop gain, 30-mW quiescent power at +3V, ±50-mA output current capability, and output voltage to within 0.5 V of either supply.

11535

Anon.
1975 INTERNATIONAL ELECTRON DEVICES MEETING TECHNICAL DIGEST. Sponsored by the IEEE Group on Electron Devices. Washington Hilton, Washington, D.C., Dec. 1-3, 1975. Cat. no. 75 CH1023-1ED

Contents:

11536

Gordon, E.I. (Bell Labs., Murray Hill, NJ)
PATHWAYS AND PITFALLS IN DEVICE LITHOGRAPHY. pp. 3-5. 1975 International Electron Devices Meeting

The device engineer, working in silicon integrated circuits, bubble memory, microwave devices and other emerging areas,consistently finds that pattern generation sets major limits on his ability to achieve higher complexity, higher performance, lower cost, greater reliability and faster design turnaround time. As a consequence major efforts are being directed to pattern generation technology. The motivation for the various activities will be examined and reviewed, and an attempt will be made to assess the relevance of these activities, pointing out potential pitfalls or areas that should be considered early in the technology development.

11537

Liechti, C.A. (Hewlett-Packard Co., Palo Alto, CA)
RECENT ADVANCES IN HIGH-FREQUENCY FIELD-EFFECT TRANSISTORS. pp. 6-10. 1975 International Electron Devices Meeting

During the 27 years since the discovery of the transistor, the advancement of transistors to higher and higher operating frequencies has been one of the most persistent objectives of semiconductor device R&D. Today, highest frequency operation and fastest switching speed are obtained from GaAs metal-semiconductor FETs (MESFETs). Above 6 GHz, MESFETs have higher gain, lower noise figure and about the same power capability as bipolar transistors. Also, p-n junction FETs (JFETs) and insulated gate FETs (IGFETs) have advanced to microwave frequencies. The cross-sections of the various high-frequency FET structures are illustrated and their performance date are listed.

11538

Kumar, R. and Ladas, C. (Motorola Semiconductor, Inc., Mesa, AZ)
CHARACTERIZATION OF PLASMA-ETCHING FOR SEMICONDUCTOR APPLICATIONS. pp. 27-28, 1975 International Electron Devices Meeting

The use of an r.f. generated plasma for the etching of dielectric and other films and for the removal ("stripping") of photoresist has become a viable alternative to the conventional, wet-chemical methods used in the fabrication of semiconductor devices. Most commercially available plasma-etchers use a CF_4 based plasma to generate atomic fluorine and can be used to etch materials like silicon nitride, doped and undoped silicon dioxide, polycrystalline silicon, single crystal silicon and certain metals.

11539

Barbe, D.F. (U.S. Navy, Nav. Res. Lab., Washington, D.C.)
CHARGE-COUPLED-DEVICE IMAGERS. pp. 60-65. 1975 International Electron Devices Meeting

The purpose of this paper is to review recent progress in visible imaging devices which use the charge-coupled concept and to discuss applications of these devices. Recent experiments have yielded experimental data on bulk trapping phenomena in buried-channel devices. Noise in CCD's is reviewed and the significance of each noise source will be discussed. Tradeoffs between high MTF versus prefiltering are formulated from an analytical point of view, and imagery is shown to elucidate the tradeoffs.

11540

Sawyer, D.E. and Berning, D.W. (Natl. Bur. of Standards, Inst. for Appl. Technol., Washington, D.C.)
LASER SCANNING OF ACTIVE SEMICONDUCTOR DEVICES. pp. 111-14. 1975 International Electron Devices Meeting

A laser scanner is described which can nondestructively explore electrical characteristics of semiconductor devices on a point-by-point basis. The results of applying the scanner to electronically map temperature distributions and hot spots in a power transistor are given. The results of mapping localized nonlinearities in electrical operation and 0.5 GHz response are also presented. Pictures show the progress of logic in a MOS shift register and demonstrate the ability to change at will the logical state of an embedded active cell with the laser.

11541

Balk, L.J., Feuerbaum, H.P., Kubalek, E. et al. (Inst. für Werkstoffe der Elektrotechnik der TWTH Aachen, West Ger.)
QUANTITATIVE DETERMINATION OF SURFACE POTENTIALS ON INTEGRATED CIRCUITS (IC) AT HIGH FREQUENCIES WITH THE SCANNING ELECTRON MICROSCOPE (SEM). pp. 115-18. 1975 International Electron Devices Meeting

An experimental set up combined with a commercial SEM is introduced, which enables the recording of stroboscopical, linearized and contrast isolated quantitative voltage contrast micrographs for frequencies up to 60MHz. This system allows the investigation of integrated circuits with a simultaneous voltage resolution of less than 100mV and a spatial resolution of 0.5µm for a maximum illuminated area of 2mmx2mm at primary beam energies between 2-30keV.

11542

Gonzales, A.J. and Powell, M.W. (Motorola Semiconductor Prod. Div., Phoenix, AZ)
INTERNAL WAVEFORM MEASUREMENTS OF THE MOS THREE-TRANSISTOR, DYNAMIC RAM USING S.E.M. STROBOSCOPIC TECHNIQUES. pp. 119-22. 1975 International Electron Devices Meeting

Stroboscopic electron beam blanking of a conventional SEM was employed to analyze high speed dynamic RAM operations. In the system described a time resolution of 20 nanoseconds was used to produce voltage contrast (V.C.) images of single events. Also the SEM was operated as a sampling oscilloscope to display timing waveforms form individual circuit nodes. Several types of 4K RAM (MCM6605) operations were analyzed to evaluate this technique in debugging MOS LSI circuits. The operations analyzed were memory cell timing waveforms, data-node storage, and node bootstrapping. The interaction of the SEM with the MCM6605 operation was also analyzed.

11543

Sredni, J. (Signetics Corp., Sunnyvale, CA)
USE OF POWER TRANSFORMATONS TO MODEL THE YIELD OF IC'S AS A FUNCTION OF ACTIVE CIRCUIT AREA. pp. 123-25. 1975 International Electron Devices Meeting

Various attempts have been made to analyze the yield of IC's as a function of active circuit area, using a models different probability distribution functions of spot defects. The purpose of this paper is to show that most of the proposed models form a family of functions which correspond to a parametric family of power transformations from yield to yield to the power λ, the parameter λ defining a particular transformation. A comparison between the power transformation approach to earlier modeling techniques will be discussed. After developing the necessary statistical theory, a simple procedure for the model building process will be presented.

11544

Lieberman, A.G. (Natl. Bur. of Standards, Inst. for Appl. Technol., Washington, D.C.)
PROBLEMS IN USING SURFACE ANALYSIS TECHNIQUES FOR THE DEPTH PROFILING OF MICROELECTRONIC MATERIALS. pp. 126-29. 1975 International Electron Devices Meeting

Practical problems associated with the depth profiling of impurity distributions in silicon and silicon dioxide are illustrated for several widely used surface analysis techniques as applied at a number of laboratories. The methods used for depth profiling were Rutherford backscattering spectroscopy, Auger electron spectroscopy X-ray photoelectron spectroscopy. The profiles measured for zinc-implanted silicon displayed good overall agreement when presented on a normalized scale, but when presented on an absolute basis displayed large discrepancies attributed to matrix effects and instrumental artifacts. An examination of some typical analysis craters by optical interferometry, stylus profilometry, and scanning electron microscopy revealed severe redeposition of the sputtered material, asymmetrical cavities with concave or convex bottoms, and severe undercutting at material interfaces.

11545

Verma, K.B. and Westlake, R.T. (Tektronix, Inc., Beaverton, OR)
A MICROWAVE HIGH VOLTAGE BIPOLAR POWER TRANSISTOR. pp. 155-58. 1975 International Electron Devices Meeting

High power microwave transistors have only recently been reported. This paper presents a high voltage microwave power transistor, which has been developed for instrument application at Tektronix, Inc. Some of the design considerations and performance data are reported. Contributing factors for the performance are indicated.

11546

Yoshida, I., Kubo, M. and Ochi, S. (Hitachi Ltd., Central Res. Lab., Kokubunji, Tokyo, Japan)
A HIGH POWER MOSFET WITH A VERTICAL DRAIN ELECTRODE AND MESHED GATE STRUCTURE. pp. 159-62. 1975 International Electron Devices Meeting

In this article a power MOSFET is described which exhibits 20A current, 300mv transconductance and 85V breakdown voltage in a $5x5mm^2$ chip. The features of the device structure are a vertical drain electrode which enables the use of most of the surface area for the source electrode and a mesh gate structure which makes it possible to increase the channel width per unit area and thereby drain current of the device can be increased. The P-channel device with an offset gate structure was fabricated from an N on P+ epitaxial wafer by using the polysilicon gate and the ion implantation processes. Stable operation of the device is possible at ambient temperatures up to 180°C.

11547

Ozawa, O., Sasaki, Y., Iwasaki, N. et al. (Toshiba R&D Center, Komukai, Kawasaki, Japan)
A 5000-CHANNEL POWER FET WITH A NEW DIFFUSED GATE STRUCTURE. pp. 163-66. 1975 International Electron Devices Meeting

This paper describes a new high power, diffused gate, vertical channel, triode-like JFET, fabricated utilizing self-aligned, heavily doped polycrystalline silicon source contacts. These techniques make it possible to realize a high source gate breakdown voltage device.

11548

Matsushita, T., Aoki, T., Otsu, T. et al. (SONY Corp., Atsugi Plant, Japan)
HIGHLY RELIABLE HIGH-VOLTAGE TRANSISTORS. pp. 167-70. 1975 International Electron Devices Meeting

The npn and pnp high-voltage transistors showing high reliabilities have been developed by using semi-insulating polycrystalline-silicon (SIPOS) films for the surface passivation. SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms. SIPOS films employed for the surface passivation of high-voltage transistors are composed of triple layers, which are oxygen-doped films of 0.5μm thickness to stabilize the silicon interface, nitrogen-doped films of 0.15μm thickness to prevent water or sodium ions from reaching the silicon surface and silicon dioxide films to prevent dielectric breakdown. The npn and pnp SIPOS transistors rated at 800 V and 2500 V have been produced in plan r-like structures with field-limiting rings. Furthermore, 10 kV SIPOS transistors with multiple rings have been fabricated and found that operation is stable.

11549

Temple, V.A.K. and Adler, M.S. (GE Corporate Res. and Dev. Center, Schenectady, NY)
A SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS. pp. 171-74. 1975 International Electron Devices Meeting

It is shown that high avalanche breakdown voltage in both plane and planar p-n junctions can be achieved by extending the heavily doped side of the junction beyond the contact and partially etching into it. This technique is capable of giving virtually ideal breakdown voltages for both plane and planar type p-n junctions and uses only a fraction of the area required for a typical negative bevel. The actual breakdown voltage depends on how carefully the etch is controlled. For planar junctions the breakdown voltages that can now be achieved are better than any previously reported. Moreover, since the technique is based on etching, mechanical contouring is avoided. The new method is illustrated both by exact calculations and by several experiments. Included in the calculations are a comparison of the new method to the 6° negative bevel for applications involving plane junctions and a comparison of the new method (for planar junctions) with the single floating field limiting ring approach.

11550

Hanson, J.W., Fordemwalt, J.N. and Huber, R.J. (U. of Utah, Inst. for Biomed. Eng., Microcircuit Lab., Salt Lake City, UT)
FABRICATION AND PERFORMANCE OF ION IMPLANTED I^2L DEVICES. pp. 281-83. 1975 International Electron Devices Meeting

Integrated injection logic devices based on vertical NPN transistors and lateral PNP injectors, and fabricated using ion-implant doping exclusively are described. Two basic processes are outlined. One uses an implanted low-energy boron pre-deposited layer, thermally driven in, to form the NPN base and p+ injectors. The other process uses high-energy implanted boron to form the active base region of the NPN device below the silicon surface. Both techniques use ion-implanted phosphorus for the n+ collectors and collars. Results of speed-power measurements for a 7-stage ringe oscillator and a 50-stage inverter string are described. The high-energy implanted boron process can be used together with Schottky-barrier collectors to further reduce the power-delay product.

11551

Cook, B., McNally, S.H. and Aung San (ITT Semiconductors, West Palm Beach, FL)
I^2L II. pp. 284-87. 1975 International Electron Devices Meeting

Present I^2L devices are limited in usable speed and current gain by the low performance of the inverse NPN transistor made with conventional bipolar processes. This report discusses new I^2L structure variations that overcome these limitations. In addition, a new process is described where the intended isolation regions are anodized to form a conduction barrier. This new I^2L II process has already yielded NPN transistors with h_{FE} = 250 and f_T = 250MHz and is expected to extend I^2L further into the high end of the speed power curve with f_T > 500MHz and propagation of 5ns.

11552

Clemens, J.T., Mowery, G.L., Doklan, R.H. et al. (Bell Telephone Labs., Inc., Allentown, PA)
A P-CHANNEL SI-GATE INTEGRATED CIRCUIT TECHNOLOGY. pp. 291-94. 1975 International Electron Devices Meeting

A general purpose p-channel Si-Gate MOS technology has been developed and characterized. The technology uses local oxidation and contains: (a) a -1.0 volt enhancement mode MOSFET, (b) a process-variable threshold voltage depletion mode MOSFET, and (c) an n/p/n process -variable gain bipolar output device. Application of the technology to beam leaded high voltage RAM circuits has created a family of special memory products for use within the Bell System. Additionally, by making use of the depletion mode MOSFET and the bipolar output device, high speed, low voltage (5 volt) TTL compatible logic circuits are realized.

11553

Clemens, J.T., Doklan, R.H. and Nolen, J.J. (Bell Telephone Labs., Inc., Allentown, PA)
AN N-CHANNEL SI-GATE INTEGRATED CIRCUIT TECHNOLOGY. pp. 299-302. 1975 International Electron Devices Meeting

A high speed, LSI, n-channel Si-Gate technology has been developed and characterized for the manufacture of integrated circuits. Utilizing the advantages of local oxidation and ion implantation, a technology is achieved which is: (a) fabricated on high resistivity Si substrates; (b) quasi-planar in topological structure; (c) completely adjustable in gate threshold voltage (enhancement and depletion modes) and field threshold voltage; and (d) highly reproducible in electrical parameter control. Additionally, by employing a thin gate insulator structure (SiO_2, 750Å) a factor of 4 increase in gain is realized with respect to standard p-channel MOSFETs. 4,096 bit dynamic RAM circuits have been designed and fabricated in this technology. Typical access times of ~50 nanoseconds with high circuit yields are realized.

11554

Rai, Y., Sasami, T. and Hasegawa, Y. (Sanyo Elec. Co., Ltd., Res. Center, Osaka, Japan)
ELECTRICALLY REPROGRAMMABLE NONVOLATILE SEMICONDUCTOR MEMORY WITH MNMoOS (METAL-NITRIDE-MOLYBDENUM-OXIDE-SILICON) STRUCTURE. p. 313-16. 1975 International Electron Devices Meeting

A new mode of operation for floating gate type electrically reprogrammable nonvolatile memory is proposed. The proposed memory has the P-channel MNOS structure with the floating molybdenum gate. This floating gate is charged positively ("WRITE") by means of non-avalanche mechanism (the Schottky emission from floating gate to the Si substrate), and charged negatively ("ERASE") by the avalanche breakdown at the source and/or drain junction. The advantage of this type of memory is that it can be operated with only negative voltages. The unit cell consists of a MNMoOS and a MNOS transistor. The method of the bit selection in the cases of "WRITE" and "ERASE" operations is explained in detail, and the fully decoded 256-bit memory array is produced with 200 Å SiO_2 and 800 Å Si_3N_4 gate structures. The typical value of the writing and that of the erasing voltage of this device are respectively -30 V and -20 V for 1 ms pulse duration.

11555

Shannon, J.M., Board, K., Brotherton, S.D. et al. (Mullard Res. Labs., Redhill, Surrey, Engl.)
CHARGE COUPLED F.E.T. DEVICES (C.C.F.F T.). pp. 320-23. 1975 International Electron Devices Meeting

A charge coupled F.E.T. array is described which gives an amplified, non-destructive measure of the size of the charge packet under each electrode of a CCD line. The basic concept uses the fact that the surface potential and consequently the depth of the depletion layer under any electrode of a CCD line is sensitive to the size of the charge packet under that electrode. As a result, an integral array of F.E.T.'s can be formed simply by changing the electrode structure of one of the phases. Results from a four bit surface channel device in an n-type layer on a p-type substrate are used to illustrate the basic properties of the device.

11556

Houston, D.E. and Krishna, S. (GE Corp. Res. and Dev. Center, Schenectady, NY) and Piccone, D. (GE Static Power Component Operation, Collingdale, PA) and Finke, R.J. and Sun, Y.S. (GE Semiconductor Prod. Dept., Auburn, NY)
FIELD CONTROLLED THYRISTOR (FCT) - A NEW COMPONENT. pp. 379-82. 1975 International Electron Devices Meeting

The Field Controlled Thyristor is a new medium power (650V, 20A) switching element. In the on condition the FCT operates as a p-i-n rectifier with a correspondingly low forward voltage drop. Conductivity modulation of the FCT's base region allows it to handle higher current densities than a power transistor with comparable voltage rating. The device owes its uniqueness to its planar gate structure.

11557

Derbenwick, G.F. and Fossum, J.G. (Sandia Labs., Albuquerque, NM)
CMOS OPTIMIZATION FOR RADIATION HARDNESS. pp. 433-36. 1975 International Electron Devices Meeting

Several approaches to the attainment of radiation-hardened MOS circuits have been investigated in the last few years. These have included implanting the SiO_2 gate insulator with aluminum using chrome-aluminum layered gate metallization, using Al_2O_3 as the gate insulator, and optimizing the MOS fabrication process. Earlier process optimization studies were restricted primarily to p-channel devices operating with negative gate biases. Since knowledge of the hardness dependence upon processing and design parameters is essential in producing hardened integrated circuits, we have undertaken a comprehensive investigation of the effects of both process and design optimization on radiation-hardened CMOS integrated circuits. The goals of our study are to define and establish a radiation-hardened processing sequence for CMOS integrated circuits and to formulate quantitative relationships between process and design parameters and the radiation hardness.

11558

Saraswat, K.C. and Meindl, J.D. (Stanford U., Dept. of Elec. Eng., Stanford, CA)
BORSENIC BIPOLAR PROCESS. pp. 437-39. 1975 International Electron Devices Meeting

A new process utilizing simultaneous diffusion of Boron and Arsenic (Borsenic) from doped oxide, to fabricate high performance bipolar transistors has been developed. The doped oxide is deposited at low temperature by oxidation of SiH_4, B_2H_6 and AsH_3. Since As diffuses much slower than B in Si, by heating the doped oxide at high temperatures n+ -p-n structures have been obtained. By varying the time and temperature of diffusion or by varying As or B content in the oxide, we have fabrication from extremely shallow (e.g. X_{EB} =0.3μ, W_{BASE} = 0.15μ) to fairly deep (e.g. X_{EB} = 2μ, W_{BASE} = 0.4μ) bipolar transistors. Details of the fabrication process and properties of the transistors are presented.

11560

Barson, F. (IBM System Prod. Div., East Fishkill, Hopewell Junction, NY)
EMITTER-COLLECTOR SHORTS IN BIPOLAR DEVICES. pp. 447-49. 1974 International Electron Devices Meeting

A number of processing defects may produce emitter-to-collector shorts in double-diffused bipolar transistors. Photolithography errors may cause lateral shorting of adjacent emitter and collector regions; or a localized masking during base diffusion can result in the absence of base region between emitter and collector (in a vertical director). Particulate contamination, especially if it contains phosphorus, can also result in localized emitter-collector shorts by overdoping the p-type base region. However, by far the most interesting, and the most troublesome, incidence of emitter-collector shorts is that due to "pipes". This paper will explore the "pipe" phenomenum and propose several theories as to their formation.

11561

Kressel, H., Ladany, I., Ettenberg, M. et al. (RCA Labs., Princeton, NJ)
RELIABILITY SEMICONDUCTOR LIGHT SOURCES FOR FIBER OPTICAL COMMUNICATIONS. pp. 477-79. 1975 International Electron Devices Meeting

This paper reviews reliability aspects of CW laser diodes and high radiance LED's. The most advanced of these devices are AlGaAs heterojunction structures designed for emission in the 8200-8600 A spectral range where most of the available fibers have the lowest transmission loss (5-10 dB/km). In CW lasers emitted power levels to about 100 mW (from one side) have been achieved. More modest power levels are obtained from LED's (1-5 mW). Excellent progress has been made in identifying and eliminating the major failure mechanisms which plagued early devices. A major failure mode is known to be caused by certain metallurgical defects in the vicinity of the p-n junction. In addition, CW laser diodes can degrade as a result of facet damage. Both of the basic failure modes have been brought under substantial control, and stable device operation for many thousands of hours is being achieved.

11562

King, F.D., SpringThorpe, A.J. and Szentesi, O.I. (Bell-Northern Res., Ottawa, Ontario, Can.)
HIGH-POWER LONG-LIVED DOUBLE HETEROSTRUCTURE LED'S FOR OPTICAL COMMUNICATIONS. pp. 480-83. 1975 International Electron Devices Meeting

The use of light emitting diodes (LED's) in optical communications systems is critically dependent on the availability of high power single fiber compatible devices capable of sustained operation for times in excess of 10^5 hours. In this paper, the design and evaluation of double heterojunction Burrus [1] type GaAlAs LED's optimized for coupling to large core multimode glass fibers is described.

11563

Simpson, J.E. and deMars, G.A. (Raytheon Res. Div., Waltham, MA)
LIFE TEST OF EBS DIODE AT 200-300 W DISSIPATION. pp. 533-36. 1975 International Electron Devices Meeting

This paper reports life test data on the highest CW power EBS device demonstrated to date. A silicon EBS diode of 60 mm^2 active area, but with only 10 mm^2 under electron bombardment, mounted on a water-cooled heat-sink, was operated at 200 to 250 W dissipation for 5000 hours. During this period, reverse leakage characteristics were stable but current gain declined in the first 1000 hours. From 5000 to 8000 hours, dissipation was raised to 300 W with a junction temperature which ultimately proved to be over 200°C. Leakage current increased substantially during this period. Cathode deterioration forced a reduction of power to 250 W after 8000 hours. The diode was short-circuited after 9360 hours by the growth of a crystalline projection outside the area of bombardment. Prior to the beginning of the life test, the diode temperature was measured in EBS operation by an infrared technique. A theoretical prediction of CW performance for EBS amplifiers is also given.

11564

Masuhara, T. and Muller, R.A. (U. of Calif., Dept. of Elec. Eng. and Computer Sci. and the Electronics Res. Lab., Berkeley, CA)
COMPLEMENTARY DMOS PROCESS FOR LSI. pp. 543-46. 1975 International Electron Devices Meeting

Through the application of diffused MOS (DMOS) transistors to the design of complementary MOS circuits, a CMOS process that is simpler and denser than that presently used has been designed and demonstrated. Test circuits using 1 ohm. cm n-type (100) silicon substrates had the following characteristics: n-channel threshold = 2 V, p-channel threshold = -2 V, $B_N/Bp = 1.7$. Single inverter and 8 stage inverter chains have successfully been operated with supplies from 3 to 8 volts.

11565

Dishman, J.M. (Bell Labs., Murray Hill, NJ)
LIMITATIONS ON THE MAXIMUM OPERATING VOLTAGE OF CMOS INTEGRATED CIRCUITS. pp. 551-54. 1975 International Electron Devices Meeting

A one-dimensional model has been developed to study the breakdown voltage behavior of an n-channel IGFET in a conventional CMOS integrated circuit. Two parasitic npn bipolar transistors intrinsic to the circuit which shunt the IGFET are found to limit the breakdown voltage below the intrinsic value of the drain/p-tub junction. Turn-on of the parasitics occurs as a result of hole avalanche current flowing in the p-tub at low-level multiplication. Semiquantitative agreement with experimental results is obtained using one adjustable parameter. The model has been used to show how lowering the resistance between the p-tub contact and the n-channel drain reduces the effect of the vertical parasitic.

11566

Sutherland, A.D. and Kennedy, D.P. (U. of Fla., Dept. of Elec. Eng., Electron Device Res. Center, Gainesville, FL)
A COMPUTER MODEL FOR LATERAL THERMAL INSTABILITIES IN POWER TRANSISTORS. pp. 569-72. 1975 International Electron Devices Meeting

The formation of hot spots is an important phenomenon accounting for the failure mechanism known as forward second breakdown in power transistors. This paper describes a computer model devised to approximate, in three spatial dimensions, the nonlinear thermo-electric feedback mechanisms producing this phenomenon. The model allows substantial flexibility in the emitter stripe topography, and includes provisions for two forms of emitter ballasting as corrective measures.

11567

Chang, F.Y. and Chang, A.W. (IBM System Prod. Div., Hopewell Junction, NY)
CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES. pp. 577-80. 1975 International Electron Devices Meeting

This paper presents a theoretical and experimental study on the isolation junction characteristics of bipolar transistors fabricated with combined oxide and diffused isolation structures. Using a quasi two-dimensional approach, the junction capacitance and junction breakdown voltage are computed as functions of device design parameters such as impurity concentration profiles and spacing between the diffusion window edges. Threshold voltage of surface inversion is also computed by taking into account the non-uniformity of the boron profiles and the boron depletion effect. Advantages and disadvantages of forming an N channel stop by reach-up and reach-down boron diffusions are compared. Experimental results are included to substantiate the theoretical results.

11568

Anon.
1974 INTERNATIONAL MICROELECTRONIC SYMPOSIUM. Sponsored by the International Society for Hybrid Microelectronics. Sheraton-Boston Hotel, Boston, MA, Oct. 21-23, 1974

Sessions:

I	Advances in Thick-and-Thin-Film Materials
II	Hybrid Components Active and Passive
III	Hybrid Manufacturing Technology
IV	Thick and Thin Film Process Control
V	Bonding and Interconnections
VI	Polymers and Hybrids
VII	Hybrid Packaging
VIII	In-Line Quality Control
IX	New Applications for Hybrids
X	Reliability Analysis
XI	Advances in Microelectronics at the University Level

11569

Mandal, R.P. (Itek Corp., Appl. Technol. Div., Sunnyvale CA)
TITANIUM NITROXIDE BURIED-LAYER THIN FILM PASSIVATION. pp. 1-6. 1974 International Microelectronic Symposium

Titanium nitroxide thin films have been deposited as the reaction product of thermally evaporated titanium metal and gaseous nitric oxide. These films have been applied to buried-layer thin film resistor passivation, in which an intermediate layer of titanium nitroxide is sandwiched between resistive and interconnection films. The resistivity of overcoated titanium nitroxide, as-deposited, remains relatively low, providing good electrical contact to underlying resistive films. However, thermal oxidation of exposed areas causes resistivity to greatly increase, forming a desirable insulating resistor passivation layer. The electrical properties of deposited titanium nitroxide films have been examined as a function of deposition and processing parameters applicable to thin film microelectronic technology. Circuit patterns were defined by means of additive techniques using metal shadow masks, in addition to conventional subtractive techniques, to aid in the investigation of film characteristics. Data on the influence of deposition and processing parameters, including deposition rate, nitric oxide gas pressure, film thickness, and oxidation time/temperatures, on electrical properties are presented.

11570

Zeien, R.H. (RCA, Solid State Technol. Center, Somerville, NJ)
CHARACTERIZATION OF THICK FILM FRITLESS METALLIZATION. pp. 7-15. 1974 International Microelectronic Symposium

A comprehensive study of thick film fritless gold and silver conductor compositions is presented. These materials were evaluated to determine processing requirements and ultimate characteristics, assembly capability and compatibility with conventional thick film material. Processing and the effects of variations on the fired film characteristics are reviewed, covering screen printing techniques and dry/fire methods. Data are presented on film thickness, resolution, density, adhesion and surface conditions as fired on 96% alumina substrates. The results of bonding tests are examined to determine the effect of variations in fabrication procedures, such as firing profiles, sequence firing and shelf life.

11571

Schneider, B., Vinikman, V. and Samuel, A. (ELTA Electronics Ind., Ltd./Israel Aircraft Ind., Ltd., Ashdod, Israel) and Kaplan, E. (Hebrew U of Jerusalem, School of Appl. Sci. & Technol., Jerusalem, Israel)
THICK-FILM MATERIAL MICROSTRUCTURE: THE INFLUENCE OF PROCESSING CONDITIONS. pp. 16-24. 1974 International Microelectronic Symposium

This paper describes an investigation into the effects of processing conditions on the microstructure of thick-film materials. Various commercially available pastes from several vendors were studied. The variables of printing, drying, and firing were evaluated for their effects on structure, as applied with equipment used at ELTA. Determination of microstructure was performed using a scanning electron microscope (SEM), which permitted sufficient resolution and depth of focus to provide a clear picture of the formation of interfaces at the cross-sectioned samples. The bulk and interfacial structure of the various materials were studied. The differences between bond formation from material to material and material to alumina were clearly observed. Correlations between the effects of processing conditions on electrical parameters were performed with respect to microstructure. Effects of microstructure on adhesion were investigated, as were effects of microstructure on the electrical parameters of sheet resistance and thermal coefficient of resistance (TCR). Finally, a comparison is made between the results obtained with the SEM and the present hypothesis for the material-structure model, along with several proposals for updating understanding of these phenomena.

11572

Cole, S.S. (Engelhard Ind., East Newark, NJ) and Wellfair, G. (Engelhard Ind. Ltd., Cinderford, Engl.)
HIGH TEMPERATURE VISCOSITY CONTROL IN MULTILAYER GLASSES - A NEW CONCEPT. pp. 25-34. 1974 International Microelectronic Symposium

Historically, viscosity of multi-layer glass systems at high temperatures has been controlled by causing crystals to precipitate, thus changing the glass composition to create a more viscous liquid. In addition, the crystals, by their presence, contribute to sluggish flow and increase glass toughness. A radically different and proven concept is discussed in this paper in which crystals are added initially to the glass formulation. The system is termed "Zero-Flow". As the temperature is increased, the crystals are partially taken into solution, thus changing the composition of the glass and increasing its viscosity. Further increases in temperature result in further crystal solution and still higher glass viscosities are produced. As a result, the higher the temperature, the more resistant to flow the glass becomes. This technique, which is incorporated in a new system of glasses, has been found to offer significant advantages in hybrid multi-layer designs.

11573

Tsen-tsou Shih (Globe-Union Inc., Matls. Res. Dept., Milwaukee, WI)
IMPROVED SILVER-PALLADIUM TERMINATION METALLIZATION FOR THICK FILM RESISTORS. pp. 35-37. 1974 International Microelectronic Symposium

This is a report on one method which was used in an attempt to reduce or eliminate the T.C.R. geometry dependence of a cermet resistor. It was found that this dependence was eliminated by modifying the composition of the silver-palladium metallization. It is believed that the modifying addition neutralizes or compensates the adverse effect of the resistor-termination interactions by doping resistor composition in the contact region.

11574

Graves, J.F. (Westinghouse Elec. Corp., Defense and Electronic Systems Center, Baltimore, MD)
PRACTICAL ASPECTS IN THE DETERMINATION OF A THICK FILM CONDUCTOR-RESISTOR SYSTEM USEFUL TO 6 GHZ. pp. 38-44. 1974 International Microelectronic Symposium

Visual, mechanical, and electrical test criteria are defined for thick film conductor and resistor materials and empirical quality and performance limits are placed upon their ranges. The conductor materials are investigated primarily for porosity line width capability, etchability, and microwave insertion loss while the resistor materials are investigated primarily for no-load thermal age, scratch resistance, voltage resistance, and print-to-print reproducibility. Thick film conductor and resistor materials useful to 6GHz and compatible with each other are discussed and the technique for reworking once-fired resistor materials by touching them up with unthinned resistor paste, refiring, and retrimming is described. Twenty-two commercially available gold thick film conductor materials and ten resistor materials are investigated. Reactively-bonded gold thick film conductor materials are shown to be particularly qualified.

11575

Hamer, D.W. (State of the Art, Inc., State College, PA)
MULTILAYER CERAMIC CAPACITOR CHIPS FOR HYBRID CIRCUITS--THE MANUFACTURING PROCESS. pp. 45-59. 1974 International Microelectronic Symposium

The purpose of this paper is to present, in detail, one specific method, and more generally, several other approaches to making ceramic multilayers. The presentation is made based on an assumption that if one knows something about how a device is made, one can use it more intelligently. It is assumed that the reader will be basically a user of capacitors, and the paper has been written with this in mind. The discussion of the several process steps includes a description of each operation, how it relates to other process steps, and how quality and performance characteristics of the capacitor can be affected. Emphasis is placed on discussing materials used and how the various process steps affect the materials. Common quality problems, how and where they are created, and approaches to solving them are also discussed.

11576

Schupp, J.E. (Airco Speer Electronics, Niagara Falls, NY)
ULTRA LOW OHM CHIP RESISTORS. pp. 67-76. 1974 International Microelectronic Symposium

Chip resistors have been designed for the very low resistance range (.25 ohm - 10 ohm). Excellent TCR (less than 150 ppm/°C), high power and close tolerance (1%) are typical of this style chip. These chips are intended for use in hybrid integrated circuits where reflow soldering techniques are employed. The unique, thick, metal-alloy film is applied using proprietary techniques, which impart good TCR and excellent stability under load and temperature. Load life testing has been evaluated up to 8 x rated power and 150°C, with catastrophic failures. The proprietary structure eliminates problems inherent in the conductor-resistor interface area, usually associated with thick-film metallurgy; it also eliminates opens caused by substrate edges, as well as minimizing the high wrap-around resistance prevalent in thick-film termination materials. Reliability of these resistors has been proven by many hours of life testing. In addition, environmental testing is being performed regularly.

11577

Brownewell, D.L. (Motorola SPD, Linear Integrated Circuits, Mesa, AZ)
SOLDER BUMP FLIP CHIP FABRICATION USING CIRCUIT LAYOUT (PART A). pp. 77-82. 1974 International Microelectronic Symposium

This paper is a joint effort by Motorola SPD and Honeywell Computer Division, where by a possible solution to a consumer problem was generated along with advancement of the flip chip device technology which could stimulate greater interest in this assembly method. The objective was to select a device which was applicable to the consumer application, create bumps with the IBM type technology on the standard wire bond pads, and then generate a substrate preparation method which could be used to attach the flip chip reliably.

11578

Waite, G.C. (Honeywell Info. Systems, Advanced Mfg. Dev., Billerica, MA)
SEMICONDUCTOR CHIP ATTACHMENT WITH SMALL BUMB FLIP CHIPS (PART B). pp. 83-87. 1974 International Microelectronic Symposium

This paper describes methods of depositing sufficient material on a Thick Film substrate to permit use of chips with reduced bump volume. Details in the paper describe the volume calculations and artwork design for deposition of solder creme by screen printing. Selection and deposition of a dielectric glaze material to limit the area of solder wetting on the substrate pads is also described. The test vehicle used in the study is a simple 2 bit counter utilizing 14MECL gates. It was fabricated in multilayer format for comparison of operating parameters between eutectic back bonded and solder reflow face bonded chips.

11579

Kakar, A.K. and Polenske, A. (Hughes Aircraft Co., Newport Beach, CA)
ON THE LASER TRIMMING OF THICK AND THIN FILM RESISTORS. pp. 110-18. 1974 International Microelectronic Symposium

This paper deals with the typical 'on-line' problems in thick and thin film resistor trimming to illustrate the situations which commonly exist. A hard look is taken at basic resistor design and layout, process control parameters and quality control criteria. Thin and thick film resistor geometries are studied as a function of electrical tolerance and desired change in resistance. The concept of worst case programming is introduced as a basic but powerful tool in a production environment. System reliability and maintenance are discussed at length to aid the interested engineer in exploring further into his particular problems.

11580

Cocca, T. and Meyer R. (Raytheon Co., West Andover, MA) and Walter, D. (Raytheon Co., Bedford, MA)
LASER TRIMMING OF THICK FILM RESISTORS FOR MILITARY APPLICATIONS. pp. 119-30. 1974 International Microelectronic Symposium

This paper describes the results of a project to determine the feasibility of using an automated laser as a production tool for the resistor trimming of thick film hybrid circuits for military applications. The experimental approach was to compare the reliability of Raytheon's standard thick film resistor abrasive trimming process to the laser trimming process. The results showed that by using a proper thick film material system, automatic laser trimming can be reliably used for military systems.

11581

Clark, R.J. (GE, Syracuse, NY) and Nakagawa, T. (Toshiba Elec. Co., Tokyo, Japan)
THE STD PROCESS -- NEW DEVELOPMENTS AND APPLICATIONS. pp. 131-44. 1974 International Microelectronic Symposium

The STD (Semiconductor-Theromplastic-Dielectric) process was originally developed at the GE Electronics Lab. in Syracuse, NY as a means for mounting and interconnecting transistor and integrated circuit chips without wire bonds. The basic requirements for hybrid integrated circuits necessitated that a more ideal interconnection system be developed, one capable of interconnecting any type of IC chip to its circuit and package in a reliable manner and at a competitive cost. It was felt that the original STD process, which has been disclosed in previous papers, had this potential. It offered many unique advantages over competitive methods. Its main strengths were: it was amenable to batch processing, it featured a compatible intermetallic system and it lent flexibility in the choice of the substrate material. This paper deals with the development of the STD Process through several different phases; it covers process descriptions, electrical and mechanical characteristics, problem areas and comparisons with other interconnecting techniques. Test vehicles are described along with potential applications.

11582

Ertel, A. (Mica Corp., Culver City, CA)
THE FABRICATION, ASSEMBLY AND TEST OF HYBRIDS ON EPOXY-FIBER GLASS SUBSTRATES. pp. 145-53. 1974 International Microelectronic Symposium

In this article a description is given of a resistor-conductor substrate and of a conductor substrate utilizing an epoxy-glass core. The subtractive etch fabrication techniques are presented. Methods of bonding semiconductor chips at low temperatures and techniques of wire bonding are detailed. Typical circuits are shown. Also described are test results of laser trimmed resistors fabricated on epoxy-glass substrates. A scanning electron microscope is utilized to show the surface appearance of trimmed resistors and the effect of the laser beam on the epoxy-glass substrate. Resistor line widths as fine as 0.03 millimeters and conductor line widths of 0.03 millimeters were used. Data and curves are presented showing the relationship of resistor size to power dissipation on the epoxy-glass substrates. Techniques and advantages of multilayered epoxy-glass microcircuits compared to ceramic are part of the presentation.

11583

Fraconville, F., Kurzweil, K. (Compagnie Honeywell Bull, Saint-Ouen, Fr.) and Stalnecker, S.G. (Microcircuit Eng. Corp., Mount Holly, NJ)
SCREEN: ESSENTIAL TOOL FOR THICK FILM PRINTING. pp. 154-63. 1974 International Microelectronic Symposium

Many variables in thick film printing were studied and described in the literature. They refer generally to paste behavior and printing conditions. A relatively neglected item in the thick film process is the stencil screen which must be of high quality for successful, repeatable printing. Different screen types will be reviewed, comparison of the metal mask versus the emulsion screen for different applications will be presented. The main characteristics and advantages of direct-emulsion type screens will be discussed in terms of screen quality control for repeatable printing with special attention to screen tension evolution during its life-time and to selection of the proper solvent for screen cleaning. The influence of various screen parameters will be documented by typical printed examples and methods of control of these parameters in production will be described.

11584

Piccoli, S.C. (Itek Corp., Appl. Technol. Div., Sunnyvale, CA)
SCANNING ELECTRON MICROSCOPY (SEM) PROCESS CONTROL OF THIN- AND THICK-FILM MICROCIRCUIT MANUFACTURE. pp. 164-72. 1974 International Microelectronic Symposium

This paper discusses the use of the SEM, or SEMography, for routine micro control of some of the processes used in making military and commercial hybrid microcircuits. These include high- and low-density conduction runs as well as high component placement densities. The SEM technique is necessary for absolute process control of certain hybrid microcircuit process parameters. Microscopes are subject to emotion, eye deficiencies, eye fatigue, sole observation and hence subjectivity. With the SEM, mass viewing is possible. Examples of the use of the SEM to reveal subtle process variances, undetectable microscopically, where process controls should be implemented, are described. These are: 1, laser trimmed resistors, 2) stacked 1-mil round aluminum bonding wire, 3) stacked ribbon wire, 4) thin-film chromium silicide sputtered process defects, 5) SEM X-ray dispersive technique to reveal out-of-control processes, 6) ultrasonic bonding tool examination during process control, and 7) auger electron spectroscopy of miniscule process variations.

11585

Tsunashima, E. (Matsushita Elec. Ind. Co., Ltd., Wireless Res. Labs., Osaka, Japan)
RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT THE RESTRICT CONDITION OF NO CURRENT-CARRYING. pp. 173-79. 1974 International Microelectronic Symposium

Thick film materials, as grazed resistor and electrode, are made use of in discrete components also, and, new fields of their application are found as voltage divider for the stabilization of high voltage supplied to cathode-ray tube; the merit of adopting grazed resistors lying in being able to obtain high allowable temperature, miniaturization of components, and long-term voltage stability. The adnormal phenomena of high voltage stability, met with in developing the high voltage divider of thick film materials, and their evaluation methods are described herein. Now, it has also been proved experimentally that there exists the phenomena that changes of resistance value occur in the status where voltages of several kV orders are applied statically with no current flowing. The long-term stability of high voltage circuits has been established by the dddition of new evaluation methods and the designing of thick film materials and high voltage dividers.

11586

Jefferson, C.F. and Thomas, C.E. (Dale Electronics, Inc., Norfolk, NE)
CALIBRATION OF THICK FILM RESISTOR PASTES BY WEIGHT. pp. 180-86. 1974 International Microelectronic Symposium

A procedures is described for the calibration of resistor pastes by weight. This procedure can be made analytical, since the problems associated with obtaining accurate thickness measurements are minimized. The task of coordinating values assigned by the vendor and values obtained in-house is simplified. When the procedure is applied to production situations, correlation between calibration values and production values can be maintained with a minimum of set-up time.

11587

Webster, R. (Honeywell Info. Systems, Boston Computer Operations, Advanced Mfg. Dev., Billerica, MA)
FINE LINE SCREEN PRINTING YIELDS AS A FUNCTION OF PHYSICAL DESIGN PARAMETERS. pp. 187-98. 1974 International Microelectronic Symposium

The current design trend in thick film hybrids is toward larger substrate size and narrower conductor lines. This paper documents the results of a study undertaken to determine the effect of line width and spacing, substrate size, and conductor length on the occurrence of common screen printing defects. Development of a screen printing test pattern and a data reduction software routine are also described. Recommendations for selection of line width/spacing and substrate size are presented.

11588

Hill, J.R. and Culp, R.E. (Martin Marietta Aerospace, Denver, CO)
RELIABILITY CONSIDERATION FOR ULTRASONIC WIRE BONDING ON THICK FILM CONDUCTORS. pp. 199-204. 1974 International Microelectronic Symposium

Aluminum ultrasonic wire bond failures were experienced in a relay driver hybrid circuit. The failures were found to be breaks at the bond heel of first bonds. Subsequent analysis showed that the bond heel breaks had a secondary relationship to the actual problem of insufficient bond strength in the immediate area of abrasive trimming. Possible solutions to this problem were evaluated and these results will be presented. One solution was selected which effectively reduced the conductor surface damage. Our experience to date has shown it has successfully provided bond strength which meet our specification requirements.

11589

DeDoskey, W.R. and Rajac, T.J. (IBM, System Dev. Div., Manassas, VA)
MECHANICAL THERMAL PULSE BONDING. pp. 205-20. 1974 International Microelectronic Symposium

Device-to-package interconnections have traditionally taken two basic forms; solder bumps and wire bonding. Solder bumps provide ganged attachment. Wire bonding is quite flexible in both design application and mechanical package aspects. But, wire bonding by either thermocompression or ultrasonics remains today a sequential wire-by-wire process. The Mechanical Thermal Pulse (MTP) process presents an opportunity to achieve a combination of the above advantages without necessarily including the disadvantages. The objective of this investigation was to determine the potential for gang attachment of aluminum leads to integrated circuit devices.

11590

Cheriff, F.J. and Salzer, T.E. (Raytheon Co., Equip. Dev. Labs., Sudbury, MA)
HIGH RELIABILITY ULTRASONIC WIRE BONDING. pp. 221-27. 1974 International Microelectronic Symposium

The Captive Line concept has proven to be an effective means for production of high-reliability components for critical defense applications. The report summarizes the technology and equipment which was developed for production of High-Rel ultrasonic wire bonds at four different Captive Line vendors. A second force channel was added to the bonding machine which aided the determination of optimized bonding parameters. Methods were developed to eliminate the transfer of vibrations originating external to the bonder to the bonding tool and to greatly reduce the amount and the effect of vibrations introduced by the motions of the bonder itself. New specifications were developed for control of wire quality and electrical and mechanical tests were developed to insure performance. In addition, a new container was developed which was both a shipping container and housing for the wire while it was stored or used on the machine.

11591

Rodrigues de Miranda, W.R. and Oswald, R.G. (Honeywell Aerospace Div., St. Petersburg, FL)
CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK AND THIN FILM GOLD. pp. 228-44. 1974 International Microelectronic Symposium

A series of tests was made to determine the effects of burn-in times and temperatures on aluminum ultrasonic wire bonds made to various thin and thick film gold conductors. Test substrates, simulating hybrid devices, consisted of alumina ceramic covered with 1) a screened-on thick film gold conductor pattern, and 2) a thin film deposited and subsequently etched gold-nickel-nichrome pattern. Resistance measurements, followed by destructive pull tests, were made on at least 25 wires on each conductor type at 0 hours, after storage at 125°C for 90 hours, respectively. Wire resistance pull strength and break point were recorded. Data was evaluated statistically and mean and standard deviation values were determined for each group. Distribution plots were made on normal probability paper to determine the percentage of low strength bonds in each group. Materials which indicated less than 0.01 percent of bond population at or below 2 grams at any of the exposure times were considered acceptable

11592

Lenhardt, B.W. and Youngberg, D.A. (Bendix Corp., Kansas City, MO)
REMOVAL OF HYBRID MICROCIRCUIT BEAM-LEAD DEVICES FOR POSTMORTEM TESTS. pp. 245-48. 1974 International Microelectronic Symposium

The assembly of hybrid microcircuits (HMC) generally utilizes the process of thermocompression bonding to attach beam-lead components to the substrate. Several reasons may dictate the need to remove and replace one or more beam-lead devices (BLD) on a hybrid. A scrape-off technique that is generally used throughout industry to remove beam-lead devices can seldom remove the beam-lead device intact and undamaged. This paper describes a technique that can successfully remove beam-lead devices from a hybrid and maintain the device integrity for postmortem tests, and that does not adversely damage substrate metallization or the hybrid circuit.

11593

Piccoli, S.C. (Itek Corp., Appl. Technol. Div., Sunnyvale, CA)
A CASE FOR BETTER EPOXY PERFORMANCE TESTING AND NEED FOR STANDARDIZED FORMULATIONS. pp. 249-55. 1974 International Microelectronic Symposium

The circuits of many microelectronic devices fail because many plastic adhesives have not been rated for actual service environment. Mechanical and electrical stressing can accelerate failure of the adhesive bond so that marginal units fail under service conditions. Chemical catalysts present can cause interaction between components and break down the epoxy bond while the device is in the assembly process after the epoxy has cured. Thermal shock can break down the adhesive properties and even cause degradation of electrical conductivity of conductive epoxies. Claims that epoxy chemistry has kept pace with electronic packaging technology are not true. Several aspects of epoxies are also discussed.

11594

Bagnall, R.T. and Schroter, S.G. (Raytheon Co., Quincy, MA)
SELECTION AND CONTROLS OF POLYMERS USED IN THE MANUFACTURE OF HYBRID CIRCUITS. pp. 256-63. 1974 International Microelectronic Symposium

Raytheon instituted a study program whose objective was to design and evaluate tests that could be used as an aid to both select and control polymers. The main areas of investigation were as follows: (1) Weight loss, (2) Conductivity, (3) Particle Size, (4) Shear Strength, (5) Bleeding, (6) Corrosion, (7) Viscosity, and (8) Shelf Life. Some Thirty epoxy materials, including conductive (silver and gold) and non-conductive polymers, were subjected to these tests. Over 400 samples were prepared and tested both initially and as function of Life. The results showed large differences in the materials and also that no one material excelled in all areas of investigation.

11595

Licari, J.J., LaChapelle, T.J., Braun, G.W. et al. (Rockwell Internatl., Autonetics, Anaheim, CA)
CONFORMAL POLYMER COATING FOR NON-LIDDED HYBRID MICROCIRCUITS. pp. 264-71. 1974 International Microelectronic Symposium

A brief review of the advantages and limitation of various polymer coatings for use on hybrid microcircuits is presented. The results of an experimental program to determine the feasibility and reliability of using a thick silicone coating as a replacement for a hermetic package are presented. Test circuits coated with 5 to 20 mils of a high purity, 100% solids, silicone successfully passed many severe environmental tests, some exceeding MIL-STD-883 requirements. Though showing promise as a low-cost packaging method, the use of polymer coatings in lieu of metallurgically sealed packages for military specifications will require further improvements and standardization in interconnection and device passivation methods. Further, more statistical data on the long-term reliability of polymer coated hybrids will be necessary.

11596

Hernandez, L. (Cutler-Hammer, AIL Div., Melville, NY)
EPOXY TECHNIQUES FOR HYBRID MICROWAVE INTEGRATED CIRCUITS. pp. 272-75. 1974 International Microelectronic Symposium

Although the use of epoxies in manufacturing hybrid microelectronics at VHF frequencies is well established, their use at microwave frequencies is not widely known. We have developed PIN diode attenuators in MIC configurations at 15 GHz and other MIC's (mixers, oscillators, medium-power amplifiers) in the 2 to 4 GHz range. We have also used epoxies on space-qualified 1-GHz MIC hardware. This paper describes some of the epoxy techniques used to produce and modify hybrid MIC's at microwave frequencies.

11597

Kasatkin, A. (Analog Devices Semiconductor, Wilmington, MA)
THE USE OF EPOXIES FOR HIGH VOLUME PRODUCTION OF MICRO ELECTRONIC COMPONENTS. pp. 276-78. 1974 International Microelectronic Symposium

Epoxies are usually selected for microelectronic applications because of their unusual combination of properties not obtainable with any other type of plastic. They posess good chemical resistance, high electrical insulation and excellent mechanical properties. In addition shrinkage is very low on curing, and the adhesive are outstanding. These resins can be used as 100% solids system. Low viscosities can be obtained without the use of solvents. Epoxy resins can be cured anywhere from room temperature up to 150°C. Since there are a multitude of different hardeners available for curing these resins, epoxies can be tailor-made to fit specific applications. This combination of properties makes the epoxy resins the most versatile plastic known today. The information presented here is directed toward those involved in or associated with packaging and sealing microcircuits.

11598

Walker, J. (Dexter Corp., Hysol Div., Industry, CA)
THE PERFORMANCE OF LIQUID EPOXY ENCAPSULANTS IN SEMICONDUCTOR APPLICATIONS. pp. 279-82. 1974 International Microelectronic Symposium

In the last five years, vast improvements have been made in the electrical, thermal, and environmental performance of epoxy based systems as semiconductor encapsulants. These improvements have been most evident and widely publicized in the molding powder products, but similar advances have occurred in the liquid products. Data is presented which illustrates the performance levels which have been achieved with liquid encapsulants and the technological advances which have made this possible are discussed. The data presented includes device performance after exposure to 85°C to 85% R.H., pressure cooker, high temperature reverse bias, thermal shock, and thermal cycling. Results on these tests are correlated with the physical properties of the epoxy encapsulant and its chemical composition

11599

Rees, G.H. (Brush Wellman Inc., Chem. Met., Prod. Dev. and Res., Elmore, OH)
PROCESSING AND PROPERTIES OF BERYLLIA SEMICONDUCTOR CARRIERS. pp. 283-92. 1974 International Microelectronic Symposium

Extreme thermal conditions are met with the use and proper design of semiconductor (chip)carriers. In a computer simulated operation of device, the θ_{j-c} is reduced from 27°C/watt for alumina to 4.8°C/watt with beryllia. Only minor modifications of alumina substrate processing are required to accommodate beryllia. Commercially available nobel metal and base metal cermet pastes, as well as refractory metallizations, yield typical adhesive strengths. Dimensional tolerances and surface quality are factors influencing metallization conditions and heat transfer. Joining considerations are discussed.

11600

Meyer, D.E. (Tex. Instr. Inc., Semiconductor Group, Mfg. Process Lab., Dallas, TX)
MEASUREMENT AND CONTROL OF ATMOSPHERE IN HERMETICALLY SEALED SEMICONDUCTOR PACKAGES. pp. 293-96. F30602-74-C-0203. 1974 International Microelectronic Symposium

The package atmosphere of a hermetically sealed semiconductor device has an effect on the device reliability, either as an indirect contributor to various failure modes or directly responsible for specific failure modes. Two common failure modes attributed to undesirable package atmospheres may be involved. One disturbs the basic electronic functions of a device junction such as inversion, channeling, charge spreading or surface leakage. The other basic mode chemically alters the physical components of the devices. A typical example is corrosion of metallization or bonds. Each of these basic modes along with the effects of moisture are investigated.

11601

Hobson, L.D. (Burr-Brown Res. Corp., Tucson, AZ)
FRUSTRATIONS OF LOW COST PACKAGING AS SEEN BY A HYBRID CIRCUIT MANUFACTURER. pp. 297-302. 1974 International Microelectronic Symposium

A program to "Build Your Own Package" was started. This paper traces some of the options reviewed and some of the frustrations endured. In the interest of both design versatility and low cost, emphasis was given to a glass and/or ceramic package. The objective was to develop a package configuration that would allow the thick film screening of resistors, crossovers, and interconnects on one surface of the package. This assembly must be compatible with eutectic and/or epoxy die attachment and either ultrasonic or thermo-compression wire bonding techniques. Completed packages must have good mechanical integrity and environmental characteristics consistent with glass or ceramic packages.

11602

Nelson, D.R. (Bendix Corp., Elec. Components Div.)
THE DESIGN OF FLEXIBILITY OF GLASS WALLED MICROELECTRONICS PACKAGES. pp. 303-05. 1974 International Microelectronic Symposium

Manufacturers and users of microelectronics circuitry have numerous alternatives for packaging and protecting their circuits. Among the choices is the glass to metal sealed flat-pack. Glass to metal sealed micropackages offer the flexibility of different lead quantities and configurations without major retooling. They also can be easily interchanged between metal base, ceramic base, and modupack designs. All this in a package that has demonstrated a consistent sealing capability of less than 1×10^{-8} cc/sec air leakage can be attractive to the potential user. Not only does he have design flexibility, but he also need not lose a large number of expensive substrates due to poor package sealing yields.

11603

Samuelson, M.O. (Martin Marietta Aerospace, Orlando, FL)
HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS THE ANSWER. pp. 306-19. 1974 International Microelectronic Symposium

This paper discusses both resistance (projection) welding of metal packages from small TO-5 cans to large round and rectangular packages and parallel seam welding and soldering of flat packs. Process development and certification, electrode design and maintenance, electrode changeover and aligment, weld schedule development and certification, process control and leak testing are discussed in detail. A unique weld schedule development technique using an isoleak diagram is explained. This paper is the results of setting up a package sealing capability in a prototype and small production facility for building hi-rel military hybrid circuits to MIL-STD-883 and MIL-M-38510 requirements. It should be of interest to anyone setting up their own sealing capability or having trouble with yield in an existing production facility.

11604

Feinstein, J.H. and Leven S.S. (Westinghouse Elec. Corp., Defense and Electronic Systems Center, Baltimore, MD)
A PRACTICAL QUALITY CONTROL PLAN FOR THE THICK FILM PROCESS. pp. 320-29. DAAB07-73-C-0326. 1974 International Microelectronic Symposium

A quality control plan for the thick film process is presented for industry review. This is a universal plan that can be adapted to the particular needs of a circuit, system, or a thick film facility. The key processing steps are individually defined, and thick film failure modes and failure mechanisms are identified. Inspection steps and procedures designed to detect and to prevent these failures are discussed. Process flow charts are provided to show the inter-relationships between the processing steps and the inspection steps.

11605

Youngberg, D.A. and Lenhardt, B.W. (Bendix Corp., Kansas City, MO)
CHARACTERIZATION OF THERMOCOMPRESSION BONDING PARAMETERS FOR BEAM-LEAD BONDING. pp. 330-35. 1974 International Microelectronic Symposium

Thermocompression (TC) bonding is a technique used to weld two similar materials by application of heat and pressure for a specific time. To obtain reliable, consistent beam-lead attachment by TC bonding, each bonding parameter value must be known and controlled. TC bonding schedules are developed to determine parameter boundary values that depend on the fundamental physics of the bonding process. This necessitates thorough TC bonder characterization (definitions of limits). This paper discusses the practical considerations of beam-lead wobble-tool bonding and describes the techniques used to characterize bonding tool temperature, work-stage temperature, bond time or wobble speed, and bond force.

11606

Pantanelli, G.P. (Bell Telephone Labs., Inc., Allentown, PA)
MEASUREMENT OF THE SOLDERABILITY OF THICK FILM CIRCUITS. pp. 336-46. 1974 International Microelectronic Symposium

A technique to obtain quantitative measurements of solderability is presented here. This technique, which is directly applicable to thick film components, measures the forces acting on a sample partially immersed in a molten solder by using a meniscometer solderability tester. The progress of wetting is followed and the time required to achieve a given degree of wetting, together with the final wetting forces give the required quantitative and non-subjective measures of the solderability or non-solderability of thick film circuits. This report shows several possible applications of this technique to the thick film soldering technology.

11607

Riemer, D.E. (Boeing Electronics, Microelectronics Div.)
DEPOSITION WEIGHT, A POWERFUL CONTROL TOOL FOR THE THICK FILM PROCESS. pp. 347-52. 1974 International Microelectronic Symposium

Thick film technology is capable of mass producing electronic components with precise mechanical dimensions. This paper is investigating the conversion of the amorphous thick film ink into electronic hardware of well defined shape. A concept is presented that is based on volume as the critical parameter of the electronic component and the thick film process. Solids content, density and deposition weight are introduced as part of the volume concept. Deposition weight is discussed as the control parameter for the screening operation which offers greater resolution, accuracy and convenience than the commonly used thickness.

11608

Ford, J.R. (Gen. Dynamics Pomona Div., Hybrid Production Facility, Pomona, CA)
SPOT - AN IN-LINE QUALITY CONTROL SYSTEM FOR HYBRID MICROELECTRONIC ASSEMBLIES. pp. 353-55. 1974 International Microelectronic Symposium

The Systematic Process Observation Technique (SPOT) is developed from a basic definition of Process Control requirements. It employs an observation method similar to "work sampling" as used by Industrial Engineering in work measurement. Emphasis is placed on a technique that is problem preventative oriented. Corrective action lag permits discrepant products to be made during the interval between problem detection and problem correction. When the preventive and corrective action controls are tied together the system becomes "closed-loop".

11609

Eisermann, D.E. and Halyard, S.M., Jr. (IBM, Manassas, VA)
CHARACTERIZATION OF POLYMERIC MATERIALS USED IN MICROELECTRONIC DEVICE BONDING. pp. 356-67. 1974 International Microelectronic Symposium

Several conductive and nonconductive epoxy systems recommended for use in microelectronic device bonding applications have been characterized by thermal analysis and analytical techniques. Data on such properties as degradation temperatures, weight changes as a function of temperature, coefficient of expansion, second-order transition temperature shrinkage behavior and pean exothermic reaction temperature of polymeric materials were determined to be important in order to optimize curing conditions for specific polymer applications. Thermal analysis has successfully been used in observing the shrinkage behavior of some conductive gold and silver filled resin systems. Fluctuating contact resistance readings in ohmic die bonds had been experienced in microelectronic packages using conductive epoxy systems, necessitating a change to eutectic die bonding for uniform ohmic contacts.

11610

Thun, R.E., Greetham, D.E. and Cserhalmi, N. (Raytheon Co., Bedford, MA)
COMPLEX BEAM-LEADED LOGIC AND MEMORY ARRAYS FOR EFFICIENT HYBRID PACKAGING. pp. 368-75. 1974 International Microelectronic Symposium

A family of digital beam-lead devices in bipolar technology is described, utilizing from 50 to 60 gold beam leads per device. The logic devices are master arrays containing from 40 to 300 gates. These arrays can be personalized easily to implement complex high-speed digital designs. A compatible family of high-speed memory devices is also provided. The entire family of devices can be utilized in thin film as well as thick film hybrid assemblies. Interconnect networks are routed by computer to achieve a short development cycle. Various functions developed for a number of military programs have amassed 6 million device hours without failure.

11611

Kocsis, A., Leroux, A., Richard, S. et al. (Université de Sherbrooke, Sherbrooke, Québec, Can.)
A THICK FILM HYBRID ELECTRONIC WATCH PROTOTYPE. pp. 376-84. 1974 International Microelectronic Symposium

Microelectronic digital wrist-watches mark a radical departure from the way man has told time for centuries, since conventional mechanical watches using a balancing wheel may have as many as 100 moving parts. In order to reduce wear and increase accuracy most of presently known electronic wrist-watches use a quartz crystal as time base. While some models are still using a stepping motor and the conventional analog rotary display, digital electronic watches have no moving parts at all. Instead they transform the oscillator frequency into a signal used to control either a LED or a liquid crystal display. In the wrist-watch we developed, as stated by the design requirements, we used a Monsanto MAN3M seven segment display. The entire electronic circuit is represented in this article.

11612

Groves, H.T. (Litton Data Systems, Van Nuys, CA)
INTEGRAL LED DISPLAY/DRIVE CIRCUIT PACKAGING. pp. 385-94. 1974 International Microelectronic Symposium

This module contains eight 35 dot alphanumeric LED arrays, with their associated drive and memory circuitry made of off-shelf CMOS devices. The package is a custom multilayer ceramic type with two separate sections, one for the drive and memory circuitry, the other for the LED display. The two sections are interconnected via buried traces in multilayer package. A new redundant LED wiring method is used on the arrays to give a reliability increase of several fold over designs using a more conventional wiring method. The section containing the drive and memory circuitry is hermetically sealed, and the LEDs in the other section are covered with a clear molded epoxy material for environmental protection.

11613

Peters, J.A. (Bendix Corp., Kansas City, MO)
AN ACTIVE LASER TRIMMER FOR PRODUCTION TRIMMING OF FUNCTIONAL HYBIRD MICROCIRCUITS. pp. 395-97. 1974 International Microelectronic Symposium

The output functions for hybrid microcircuits are required to be within one percent or better of design value. A computer-controlled YAG laser trimmer was developed to increase the resistance of the deposited resistors that control output such as voltage, current, frequency, and time interval. The computer program contains information on each circuit transfer function and each related trim resistor to predict the required cut length. This system makes use of repetitive sampling during a short interval when power is applied to the circuit, and trimming is performed during a much longer interval when power is off. This provides for rapid trimming of functions with short duty cycles. Early results show that the active laser trimmer is a satisfactory production method for obtaining close-tolerance electrical functions.

11614

Richardson, T.W. and Parks, P.F. (Electro Sci. Ind., Inc., Portland, OR)
A METHOD OF OBTAINING OPTIMUM TRIMMING PERFORMANCE FROM A LASER SYSTEM. pp. 398-401. 1974 International Microelectronic Symposium

The resources available for achieving requirements placed on laser resistor trimming are usually limited to the laser system itself, a microscope and the operator. This paper describes a method of using these resources to achieve resistor trimming specifications. The laser system is used to achieve optimum target values and short-term room temperature stability. This is done by programming laser power, Q-switch repetition rate, cutting speed, types of trim, target values and types of measurements used. The microscope is used in conjunction with the laser system to assure cleanliness and other physical aspects of the kerf, and to assure that trim paths remain within geometrical requirements.

11615

Michel, B. (L.T.T. Co., Fr.)
HIGH RELIABILITY COMPLEX HYBRID INTEGRATED CIRCUITS. pp. 402-04. 1974 International Microelectronic Symposium

This paper summarizes a study made on the mounting techniques being used to produce complex hybrid integrated circuits. The purpose of the study was to develop higher reliability for these circuits. In the study, products made by different processes were submitted to mechanical and thermal stresses to determine their tolerance limits. Each manufacturing process was qualified, and a qualifying procedure was specified for each component used in the circuits. To verify the reliability obtained with these techniques, an accelerated life-test program was conducted in which 326 circuits were submitted to typical operating conditions for 10,000 hours at a temperature of 70 degrees C. The failure rate was 0.3×10^{-6}/h. Variation in the ceramic capacitors were shown to be the main cause of failure. The failure rate for these components was estimated to be 1.35×10^{-7}/h under a more severe qualifying procedure.

11616

Szekely, G.S.
MEASUREMENT ACCURACY, PRECISION AND REPEATABILITY WITH RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS. pp. 405-10. 1974 International Microelectronic Symposium

Profit or loss, meeting or slipping delivery schedules, passing or failing source inspection, and numerous other woes are intimately tied up with what is and what isn't known about "accuracy", "precision", "repeatability" and "allowable instrument errors" in electrical-measurement processes. This article will explain the meaning of twelve important terms labeled Basic Considerations, including those of "systematic error", "random error", "electrical accuracy", "sensitivity", and others. Special attention is devoted to thermal, aging, and contact effects in dc measurements, using both torque-type and digital meters. Under the heading of "Practical Application", the error contributions from current forcing and from voltage measuring are calculated, as referred to a real-life example of an automated system for testing IC's. These are supplemented by a tabulated linear summation of the worst-case aggregates of all existing uncertainties the user of such a test system must face. Accuracy versus precision are further illustrated.

11617

Slaughter, E. (Singer Kearfott Div., Wayne, NJ)
HYBRID RELIABILITY. pp. 411-17. 1974 International Microelectronic Symposium

Although there is an intrinsic reliability improvement with the use of hybrid microelectronic devices over an equivalent discrete component part circuit; reliability is not necessarily inherent in the hybrid circuit unless proper care has been exercised in the development and build of the hybrids. A historical review of hybrid usage over the past five years has shown conclusively that there must be certain established controls in the design phase as well as the build phase to assure reliable devices. Data from some 200,000 hybrids have been analyzed to determine their reliability or failure history versus the depth of control exercised by the user over the manufacturing source during this period.

11618

Sulouff, R.E. (Martin Marietta Aerospace, Orlando, FL)
TIME DEPENDENT RELATIONSHIPS IN SOLDER INTERCONNECTIONS. pp. 418-26. 1974 International Microelectronic Symposium

The leaching of thick film materials by solder is recognized as a manufacturing and reliability problem. This paper develops the time dependent relationships of adhesion for platinum-gold pads soldered with tin based (95% Sn-5% Ag) and lead based (97.5% Pb-1.5% Ag-1.0% Sn) solder. The mathematical correlation of time and temperature to intermetallic growth is derived. The intermetallic formation and its relation to loss of adhesion is developed through mechanical testing and metallurgical investigation. The failed surfaces and metallurgical sections are investigated with a scanning electron microscope and energy dispersive x-ray analyzer to identify adhesion factors and intermediate phases. The loss of adhesion prior to complete transformation of the platinum-gold to intermetallic compounds is theorized to be due to the tensile forces introduced by the growth of the intermetallics. The 'self-rising' effect pulls the glass frit system and results in a mechanical loading.

11619

Lasch, K.B. and Lynch, K.S. (Raytheon Co., Missile Systems Div., Burlington, MA)
INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK FILM METALLIZATION ON CERAMIC SUBSTRATES. pp. 427-40. 1974 International Microelectronic Symposium

Solder joints connecting nickel ribbon leads to thick film metallization on ceramic substrates have been visually characterized and their strengths measured. A direct correlation was found between solder joint fillet height and strength. Changes in the visual appearance and strengths of the solder joints resulting from thermal aging have been experimentally investigated. Metallography has shown that solder joint strength degradation is accompanied by the formation of two new regions; one at the solder/thick film interface consisting of gold, platinum, tin, and palladium, and another at the solder/nickel lead interface consisting of nickel and tin. Quantitative data is presented showing the solder joint strength as a function of exposure time at three different temperatures: 100°C, 125°C and 150°C . By extrapolation, solder joint degradation rates are obtained for more benigh conditions: 0.6 lbs./year at 40°C from an initial strength of 4 lbs.

11620

Pirie, G.D. (Boeing Electronics, Microelectronics Div.)
ELECTRICAL SCREEN FOR HIGH RELIABILITY HYBRID CIRCUITS. pp. 441-49. 1974 International Microelectronic Symposium

The work described in this paper was undertaken to develop a screening method that would allow evaluation of the interrelated effects of a large number of components functioning as a unit to replace the traditional component screening techniques. In order to do this we have borrowed some techniques from the measurement industry, combined them with automatic testing, data reduction, statistics and data printout to provide an efficient cost effective method of achieving a measure of the reliability required for extreme applications, both from an individual unit and lot acceptance point of view.

11621

Mazenko, J.J. (Hughes Aircraft Co., Fullerton, CA)
THE RELIABILITY OF BEAM LEAD SEALED JUNCTION DEVICES. pp. 450-59. F30602-73-C-0204. 1974 International Microelectronic Symposium

Preliminary results will be reported on a study in which over 3,000 beam lead I.C. devices, consisting of two digital and two analog types from four major beam lead device manufacturers, were characterized electrically and mechanically, sub-divided into hermetic and non-hermetic groups, and subjected to stress tests and life tests per MIL-STD-883.

11622

Johnson, G.W. and Henderson, H.T. (U. of Cincinnati, Dept. of Elec. Eng., Solid State Electronics Lab., Cincinnati, OH)
ATTENUATED TOTAL INFRARED INTERNAL REFLECTION FOR CHARACTERIZATION OF ELECTRONIC FILMS. pp. 460-68. 1974 International Microelectronic Symposium

Attenuated Total Reflection (ATR) infrared spectroscopy utilizes the evanescent non-traveling wave which penetrates or tunnels into a completely reflecting barrier. If a finite and characteristic extinction coefficient exists in the surface film or material, energy will be absorbed at or near the characteristic frequency of the surface layer. In this way the surface layer can be sampled and characterized from the substrate side as to composition and structure near the interface (over a range of a several hundre angstroms), although the surface film may be opaque for normal transmission spectroscopy. Further, a selective sampling is possible for the state of the critical film-interface region. This method is then extended to the study of various thick film pastes, common to the hybrid electronics industry. These initial studies suggest that ATR is capable of putting some analytical science into a primarily empirical area and possibly predicting electrical and thermal stability by non-destructive chemical characterization of the film-substrate interface.

11623

Patel, D.N. and Williams, L., Jr. (N.C. A&T State U., Elec. Eng. Dept., Greensboro, NC)
METALLIC OXIDE SWITCHES USING THICK FILM TECHNOLOGY. pp. 477-85. NGR 34-012-004. 1974 International Microelectronic Symposium

Metallic oxide thick film switches were processed on alumina substrates using thick film technology. Vanadium pentoxide in powder form was mixed with other oxides e.g., barium, strontium copper and glass frit, ground to a fine powder in a micromill and pastes and screen printable inks were made using commercial conductive vehicles and appropriate thinners. Some switching devices were processed by conventional screen printing and firing of the inks and commercial cermet conductor terminals on 96% alumina substrates while other were made by applying small beads or "dots" of the pastes between tiny platinum wires. Processing involved heat treatment at varying temperatures up to 1000 degrees C in vacuum, argon, reducing atmospheres, and air firing in a tunnel kiln. Resistance - temperature tests showed resistance changes by factors of 1000 to 10,000 at various critical temperatures between 50 to 90 degrees C. Static and dynamic volt-ampere and pulse tests performed indicate that the switching and self oscillatory characteristics of these devices could make them useful in memory element, oscillator, automatic control applications, etc.

11625

Condra, L.W. (Bell Labs., North Andover, MA) and Svitak, J.J. (Western Elec. Co., Princeton, NJ) and Pense, A.W. (Leheigh U., Bethlehem, PA)
THE HIGH TEMPERATURE DEFORMATION PROPERTIES OF GOLD AND THERMOCOMPRESSION BONDING. IEEE Trans. on Parts, Hybrid and Packaging PHP-11, no. 4,290-96, Dec. 1975

The flow stress of a high purity gold has been determined so that the contribution of plastic flow to the gold-gold thermocompression bonding process can be evaluated. These compression tests at 25°C, 158°C, 311°C and 458°C indicate that for deformations over 15% the flow stress and the work hardening coefficient decrease rapidly with increasing temperature. Correlation of the compression test results and beam leads bonding experience indicates that high purity golds having a hardness of about 30 DPH would be expected to reach a steady state uniaxial flow stress of 70-90 MPa (10,000-13,000 psi) when deformed during bonding at 300°C.

11626

Rideout, V.L. (IBM)
THERMAL OXIDE ISOLATION PROCESS FOR HIGH-DENSITY MEMORIES. IBM Tech. Disclosure Bull. 17, no. 10, Mar. 1975

In the conventional 5-mask recessed oxide-modified process for 1-device memories, thermal oxide is grown over the poly-Si plate, Si bit line, and Si storage node to electrically isolate the Al word line from the cell. During this oxide growth, Si in the region of the bit line is consumed.

11627

Cromer, E.G.
AUTOMATIC TESTING OF INCOMING DIGITAL DEVICES. Electronic Packaging and Production 15, no. 2, 7 pp., Feb. 1975

As a class, digital devices represent probably one of the largest families of active components consumed by the electronics industry today, and their applications are still increasing. The user, who must test these devices at incoming inspection, often finds that they present difficult test problems. However, techniques and equipment are available for testing them, both adequately and economically.

11628

Bess, M. (N.L. Ind., Highstown, NJ)
Oswald, R. and Ohring, M. (Stevens Inst. of Technol., Dept. of Met., Hoboken, NJ)
CONTACT POTENTIAL MEASUREMENTS ON THIN SiO_2 FILMS. Solid-State Electronics 17, no. 8,813-17, Aug. 1974

Contact potential measurements by the Kelvin method were performed in vacuum on silicon wafers whose thermal oxide film was etched into the shape of a wedge. A given position along the oxide corresponded directly to a given depth and by scanning a reference electrode stripe across the wafer, information about the distribution of the oxide charge through the thickness was obtained. It was found that the oxide charge was positive and concentrated within a few hundered angstroms of the $Si-SiO_2$ interface.

11629

Poponiak, M.R., Schwenker, R.O. and Yeh, T.H. (IBM)
DIELECTRIC ISOLATION OF SILICON REGIONS. IBM Tech. Disclosure Bull. 17, no. 5, Oct. 1974

This process, utilizing anodisation of selected regions followed by oxidation of the resultant porous silicon, produces complete isolation of monocrystalline regions supported on a semiconductor substrate.

11630

Anon.
MICROELECTRONICS BUYER'S GUIDE. Electronic Packaging and Production 15, no. 11, 23 pp., Nov. 1975

The Microelectronics Buyer's Guide lists manufacturers and suppliers of various types of Semiconductor and Processing products and services. The items are listed alphabetically within the following categories:

1. Production Equipment, Tools and Accessories
2. Production Materials and Chemicals
3. Processing and Packaging Services
4. Process and Assembly Test Equipment

Addresses for each of companies listed in the buyers guide can be found in the "Alphabetical Reference of Companies Listed" immediately following the product listings.

11631

Harris, S. and Wagner, D. (Analog Devices, Inc., Norwood, MA)
LASER TRIMMING ON THE CHIP. Electronic Packaging and Production 15, no. 2, 5 pp., Feb. 1975

The functional trimming capability has long been a major processing advantage enjoyed by hybrid circuits. Now, active substrate trimming of thin-film resistors directly on the silicon chip makes functional trimming of monolithics a reality.

11632

Beeler, J.
SCREENPRINTING THICK-FILM. Circuits Mfg. 15, no. 6, 32-33, May 1975

Until metallic solutions enter the marketplace in commercial quantities, ink users should observe one of two simple procedures for dispersing powder and mixing solutions. One process consists of wetting the organic powder with a solvent and dissolving the resins in a slurry or mixing the slurry into concentrated resin solutions. A second method prescribes mixing the inorganic powder with a resin solution or plasticizer, allowing it to stand for 24 hours and slowly pouring the mixture into a film-former while stirring.

11633

Anon.
TESTING. Circuits Mfg. 15, no. 6, 36-38, May 1975

From the medley of available test equipment, these instruments and systems check and evaluate components, ICs, PC cards and assemblies.

11634

Anon.
BONDING. Circuits Mfg. 15, no. 6, 34-35, May 1975

Most of the companies represented here and many that are on the manufacturer and dealer listings in this issue, supply complete lines of machines and accessories to the electronics and microelectronics marketplace.

11635

U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Inst. for Appl. Technol., Washington, D.C.
SEMICONDUCTOR MEASUREMENT TECHNOLOGY: SPREADING RESISTANCE SYMPOSIUM. Rept. no. NBS SP 400-10. Co-sponsored by this Bureau and Committee F-1 of the American Society for Testing and Materials, National Bureau of Standards. Gaithersburg, MD., 293 pp., June 13-14, 1974

Contents:

11636

Assour, J. (RCA Solid State Div., NJ)
EFFECTS OF OXYGEN AND GOLD ON SILICON POWER DEVICES. pp. 201-08. 1974 Spreading Resistance Symposium

Several important features that make the two-probes spreading resistance tehcnique a unique process control tool for designing and manufacturing silicon power devices are elucidated in terms of the effects of electrically active oxygen and gold centers on the characteristics of transistors, thyristors, and rectifiers. The effectiveness of the spreading resistance technique is compared to other commonly practiced techniques for the investigation of diffusion mechanisms of oxygen in homotaxial NPN transistors and of gold in fast switching rectifiers and thyristors.

11637

Naiman, M.L. (M.I.T., Lincoln Lab., Lexington, MA)
POLYCRYSTALLINE SILICON ISOLATION FOR INTEGRATED CIRCUITS. Paper no. MS-3680A, 12 pp., Apr. 1974

Very high resistivity polycrystalline isolation has been successfully grown simultaneously with normally doped epitaxial collectors. Unlike previous techniques, the poly itself effectively provides dielectric isolation, resulting in low capacitance and reduced spacing. Processing is significantly simplified by using the buried layer mask for nucleation, thus eliminating the isolation step altogether. The result is a simultaneous improvement in performance and cost. Additional advantages may accrue by using the high diffusivity in poly to combine base and resistor fabrication steps. Polycrystalline silicon for isolation is characterized.

11638

Wessels, B.W. (GE, Corporate Res. and Dev., Schenectady, NY)
VAPOR DEPOSITION OF GaP FOR HIGH-EFFICIENCY YELLOW SOLID-STATE LAMPS. Reprinted from J. of the Electrochem. Soc. 122, no. 3, 402-06., Mar. 1975

Nitrogen-doped gallium phosphide has been epitaxially deposited on GaP substrates by chemical vapor deposition using phosphine, hydrogen chloride, and gallium as reactants. The morphology of the epitaxial layers and the electroluminescence of the Zn-diffused diodes were investigated as a function of substrate temperature, Ga source temperature, and reactant concentration. It was found that by decreasing the PH_3/Ga Cl ratio at which the material was grown, the electroluminescence of the diodes prepared from the material shifted to longer wavelengths as a result of increased nitrogen incorporation. Quantum efficiencies for the encapsulated yellow light emitting diodes with a mesa structure were as high as 0.15% at 20 A/cm^2 and 0.24% under pulsed operation at 100 A/cm^2.

11639

Wilson, R.G. and Long, R.L., Jr. (Hughes Aircraft Co., Hughes Res. Labs., Malibu, CA)
INTEGRATED CIRCUIT RELIABILITY AND MANUFACTURING SCIENCE (ICRMS). Final Rept., Mar. 12-Oct. 12,1973, 239 pp., Nov. 1973. AD/B002 804L. N00039-73-C-0059

The objective of this study program was to develop a technical plan and an investment strategy for the Department of Defense (DoD) that will result in improvement of the processing yield (75% goal), increase the reliability (10^{-8}/h goal), reduce the cost, and maintain or improve the performance of LSI circuits for DoD applications. Some considerations in achieving this objective involved improvement in LSI manufacturing by introducing better understanding (science into manufacturing, reduction of human skill or art and judgment in processing, using manufacturing techniques that will inherently increase reliability, reduction of screening as a means of achieving reliability, and by providing a variable product capability with a standard process to provide the modest volume, custom LSI circuit needs of DoD.

11640

Philofsky, E. and Hall, E.L. (Motorola Semiconductor Prod. Div., Matls. Res. Lab., Phoenix, AZ)
A REVIEW OF THE LIMITATIONS OF ALUMINUM THIN FILMS ON SEMICONDUCTOR DEVICES. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 4, 281-90, Dec. 1975

This paper reviews several time dependent reliability limitations of aluminum thin film metallization used on semiconductor devices. For each of the degradation modes, the present level of understanding as well as engineering data are presented. First, interactions of aluminum with the underlying silicon substrate, with silicon dioxide, and with gold are discussed. Then the time dependent degradation phenomena of electromigration, surface reconstruction, and corrosion are reviewed. A good understanding of all these limitations is important in the construction of reliable devices using this metallization.

11641

Mehta, D.A. (Western Elec. Co., Allentown, PA) and Butler, S.R. and Feigl, F.J. (Lehigh U., Bethlehem, PA)
EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE TRAPPING IN CVD Al_2O_3 FILMS ON Si. J. of Electrochem. Soc.: Solid-State Sci. and Technol. 120, no. 12, 1707-14, Dec. 1973

Al_2O_3 films, 200 nm thick, were chemically vapor deposited on (100) silicon substrates by hydrolysis of $AlCl_3$ at 900°C in a H_2-rich atmosphere of H_2 and CO_2. Heat-treatment in H_2 atmosphere produces no change in the charge state of the oxide. Heat-treatment in O_2, N_2 or Ar atmospheres produces only a redistribution of the negative charge grown in during deposition. Heat-treatment in H_2 subsequent to that in O_2, N_2, or Ar restores the original charge distribution. The flat band voltage characterizing these shifts approached a constant value with time (10V). The temperature dependence of the rate of approach to saturation is consistent with first-order kinetics and an activation energy of 1.42 eV. These results and the effects of annealing on optically active charge trapping centers are due to a hydrogen-related species formed during film deposition.

11642

Szedon, J.R. (Westinghouse Elec. Corp., Res. Labs., Pittsburgh, PA)
AN APPROACH FOR EVALUATING POLYMER MATERIALS AS PROTECTIVE COATINGS ON HYBRID MICROCIRCUITS. IEEE Trans. on Parts, Hybrids, and Packaging PHP-10, no. 4, 215-57, Dec. 1974. DAAB07-72-C-0217

Results are discussed of an evaluation program for polymer materials considered for applications as protective coatings on hybrid microcircuits. The general organization of the program was in terms of seven potential mechanisms by which coatings could fail to provide protection. Emphasis is on describing those six tests which developed differences in material behavior considered to be significant in terms of the general application. Three involved electrical performance of the films alone or in conjunction with hybrid circuit elements, two dealt with mechanical properties, and one with chemically related behavior. It is suggested that the tests could be used in selecting promising candidates for particular applications which relate to the test conditions or in understanding some failure modes which could be expected in complex hybrid microcircuit assemblies. A brief review is given of those tests which were not considered to develop distinctions between materials. As a point of exception, the role of organic coatings on bare semiconductor device surfaces was not investigated.

11643

Sproul, M.E. and Nassibian, A.G. (U. of Western Austral., Dept. of Elec. and Electronic Eng., Nedlands, Austral.)
EFFECT OF O^+ IMPLANTATION ON SILICON-SILICON DIOXIDE INTERFACE PROPERTIES. Solid State Electronics 17, no. 6, 577-82, June 1974

A detailed investigation has been made by the MOS capacitance method, into the mechanism by which fixed positive surface state charge, due to silicon rich oxide near $Si-SiO_2$ interface, is controlled by O^+ implantation into the oxide near the $Si-SiO_2$ interface, and subsequent heat treatment. High dosage implantation of 3×10^{14} O^+ ions cm^2 results in damage in oxide which is cured by 450°C annealing. However, low dosage implantation of 3×10^{12} O^+ ions cm^2 produces no detectable damage in the oxide, and increases the effective positive charge in the oxide at $Si-SiO_2$ interface. It is shown that prolonged 450°C heat treatment of O^+ ion implanted oxides results in an oxygen-silicon reaction in the silicon enriched oxide layer and reduces the fixed positive surface state charge. Subsequent heat treatments at 838°C increase the positive surface state charge to the original pre-ion implantation values, hence converting the oxide into the original silicon rich condition.

11644

Lloyd, R.A. and Hardesty, S.J. (Westinghouse Elec. Corp., Hunt Valley, MD)
INFRARED SIGNATURES FOR THE ANALYSIS OF DIGITAL CIRCUITS. pp. 7-16. A74-13803. Automatic Support Systems for Advanced Maintainability: 1973 International Symposium Record. Arlington, TX., Nov. 5-7, 1973

This paper describes studies in the use of infrared profiles of circuit elements to distinguish normal circuit operation, from abnormal operation, in a contactless technique that eliminates the node accessibility problem. All circuit faults purposely injected were able to be isolated to an area and component(s). Basic total test system concepts, utilizing this sensing technique, are also discussed.

11646

Dzimianski, J.W. (Westinghouse Elec. Corp., Systems Dev. Div., Baltimore, MD)
NMOS RELIABILITY AND PROCESS RESEARCH. Rept. no. ECOM-74-0588-1, Interim Rept., June 30-Dec. 31, 1974, 43 pp., Mar. 1975. DAAB07-74-C-0588

The objective of this report has been to establish methods for the evaluation and prediction of failure rates in NMOS BORAM memory chips. The program goals include accelerated life testing of memory and test pattern chips from the same wafers, and analysis of devices that fail during test to identify mechanisms that can lead to short or long term failure modes. Derived information will provide process research feeback aimed at improving fabrication yields and at eliminating or reducing the failure modes detected. Burn-in and load boards were prepared for 125°C, 150°C, and 200°C testing of devices with dc bias for 125°C testing of memory chips with clear/write/read excitation. Electronics for generating the clear/write/read pulses was designed and constructed. A total of 500 hours of test time at 125°C with dc bias applied was accumulated on one set of BORAM memory chips and on one set of test patterns.

11647

Leven, S.S. and Feinstein, J.H. (Westinghouse Elec. Corp., Baltimore, MD)
QUALIFICATION REQUIREMENTS FOR THICK FILM NETWORKS. Rept. no. ECOM-0326-1, Semi-Ann. Rept. no. 1, July 1-Dec. 31, 1973, 72 pp., May 1974. AD 919 961L. DAAB07-73-C-0326

A study is being conducted for the purpose of identifying controls that a thick film user may impose upon a thick film circuit supplier that will ensure a quality product with reasonable yields. This report summarizes, in addition to the method of approach, the thick film manufacturing process and recommended inspection points. Descriptions of the experiments to be performed for the purpose of developing screening procedures are included. Finally, additional areas of investigation that are of interest to the general subject of thick film quality control but beyond the scope of the present contract are also briefly described.

11648

Gerber, R.M. and Dzimianski, J.W. (Westinghouse Defense and Electronic Systems Center, Advanced Technol. Labs., Baltimore, MD)
USE OF AN ION MICROPROBE IN SEMICONDUCTOR FAILURE ANALYSIS. J. of Vacuum Sci. & Technol. 10, no. 6. 1072-73, Nov./Dec. 1973

Causes of high-ohmic contact resistance were explored by analyzing several integreated circuit samples with an ion microprobe. Presence of oxide and dopant depletion at the interface are indicated. Mapping of oxygen vs depth through an oxide revealed that not only the elements present, but also the layered structure of the material could be observed. The possible production of articles due to electrostatic charges on the surfaces of a sample was noted.

11649

Maxwell, D.A. (Westinghouse Corp., Newbury Park, CA) and Beeson, R.H. and Allison, D.F. (Signetics Corp., Sunnyvale, CA)
THE MINIMIZATION OF PARASITICS IN INTEGRATED CIRCUITS BY DIELECTRIC ISOLATION. IEEE Trans. on Electron Devices ED-12, 20-25, Jan 1965

A radically new technique for the fabrication of integrated circuits which completely changes microelectronic design is described. In place of the back-biased pn junctions usually used for isolation of devices in a substrate, a dielectric is substituted whose properties are such that almost total isolation is achieved with no increase in area. Great flexibility in the design of components is achieved through the ability to place highly conductive "wells" where needed to obtain the benefits of epitaxial techniques, and by the ability to use devices having higher breakdown voltages. The technique makes practically all circuit configurations possible, and greatly enhances the possibilities for fabrication of npn and pnp transistors in the same substrate.

11650

van Pul, B. (Motorola, Inc., Semiconductor Prod. Div., Phoenix, AZ)
MANUFACTURING METHODS, TECHNIQUES AND AUTOMATED CONTROLS FOR THE CONTINUOUS EPITAXIAL PROCESSING OF SILICON INTEGRATED CIRCUITS. Rept. no. AFML-IR-512-1(I), Interim Rept. no. 1, Nov. 1, 1971-Jan. 31, 1972, 47 pp., Apr. 1972
Rept. no. AFML-IR-512-1(II), Interim Rept. no. 2, Feb. 1-Aug. 31, 1972, 52 pp., Nov. 1972
Rept. no. AFML-IR-512-1(III), Interim Rept. no. 3, Sept. 1, 1972-Feb. 1, 1973, 31 pp., May 1973
Rept. no. AFML-TR-512-1(IV), Interim Rept. no. 4, Feb. 1-Aug. 1, 1973, 52 pp., Sept. 1973
Rept. no. AFML-TR-512-1(V), Interim Rept. no. 5, Aug. 1, 1973-Feb. 1, 1974, 41 pp., Mar. 1974
Rept. no. AFML-IR-512-1(VI), Interim Rept. no. 6, Feb. 1, 1974-Feb. 1, 1975, 44pp., Mar. 1975. F33615-72-C-1242

In this contract, Motorola will develop and implement an automated system for the epitaxial deposition of silicon on silicon wafers. The system will be under supervisory control of a computer and will operate without intervention. The contract requires the following automated functions: cleaning station, surface inspection for contamination, reactor station, and evaluation station for electrical and physical characteristics. A goal will be to provide all wafers with pertinent data from the computer memory at the end of the process. The accomplishments of these volumes are as follows:

I) Systems engineering of the basic concepts.
II) Finalization of systems engineering and initiation of mechanical design.
III) Mechanical and electrical design. Software design was initiated after the module designs attained enough basis to permit flow charting of the decision paths.
IV) Mechanical and electrical design has been completed; software design has been partially completed.
V) Procurement of parts, and mechanical and electrical assembly.
VI) Implementation of all mechanical, pneumatic and electronic hardware (except the decoder) has been completed. Computer programs were tested, and system runs made. Reactor runs were made. Further effort is required to reduce MTBF.

11651

Mikoshiba, H. and Murase, K. (Nippon Elec. Co., Ltd., IC Div., Kawasaki, Japan)
DEPENDENCE OF SILICON NITRIDE FILM THICKNESS ON BIPOLAR TRANSISTOR CHARACTERISTICS. 3 pp.

It is well known that thermal stress is induced in silicon slices during thermal oxidation, due to the difference of thermal expansion rate between silicon and silicon dioxide. This stress presumably causes the degradation of electrical characteristics of silicon devices. The stress thus induced, however, can be reduced by deposition of an appropriate film such as Si_3N_4 sealed bipolar transistors with respect to thermal stress relaxation.

11652

Horninger, K. (Siemens AG, Munich, Ger.)
FULLY DECODED MNOS STORAGE ARRAYS IN ESFI MOS TECHNOLOGY. IEEE J. of Solid-State Circuits SC-9, no. 5, 444-46, Dec. 1974

The operation of MNOS memory transistors realized in thin epitaxial silicon films on insulators (ESFI) is described for writing, erasing, and reading, and their behavior is explained by means of the so-called storage characteristics. From exploratory matrices with 2 x 2 elements the expected data of a 4-kbit chip are estimated.

11653

Ramachandran, K.N. and Cox, C.D. (Semco Instr. Co., Ontario, Can.)
INVESTIGATION OF SURFACE OXIDE LAYERS BY X-RAY APPEARANCE POTENTIAL SPECTROSCOPY. J. of the Electrochem. Soc. 121, no. 5, 673-5, May 1974

X-ray appearance potential spectroscopy using low energy electron excitation is a simple method for surface analysis sensitive to light elements. The spectra obtained from many elements show considerable structure which is presumably related to the valence band distribution. The apparatus consisted of a tungsten filament electron source and a large area, windowless, soft x-ray detector based on the photoelectric yield of a gold surface. The specimen, electron source, and a detector were located in an all metal, bakeable vacuum system having demountable, gold wire sealed flanges. Facilities were provided for surface cleaning by ion bombardment and heating the specimen in situ. A 10Å layer of oxygen on nickel was readily detected using an electron current of 2 mA. The $L_{3,2}$ structure of iron in pure and known oxide forms was obtained by performing in situ oxidation of a pure iron specimen Slight but reproducible changes in the structure were observed, indicating the potential capability of the technique to distinguish between different valence states of an element. The oxygen K spectrum also showed a multiple peaked structure.

11654

Sowell, R.R., Cuthrell, R.E., Mattox, D.M. et al. (Sandia Labs., Albuquerque, NM)
SURFACE CLEANING BY ULTRAVIOLET RADIATION. J. of Vacuum Sci. & Technol. 11, no. 1, 474-75, Jan./Feb. 1974

In summary, we have found that exposure of a metal (gold) or ceramic (glass) surface to ultraviolet radiation for a prolonged time in air (oxygen) will remove adsorbed hydrocarbon contaminants. If stored under uv radiation, a surface will not recontaminate with hydrocarbons in a normal laboratory environment. It is suggested that this cleaning/storage technique may be applicable to laboratory/production processing if proper precautions are taken.

11655

Hollar, E.L., Rebarchik, F.N. and Mattox, D.M. (Sandia Labs., Albuquerque, NM)
COMPOSITE FILM METALLIZING FOR CERAMICS. J. of the Electrochem. Soc. 117, no. 11, 1461-62, Nov. 1970

There are two primary approaches to forming a solderable/brazable surface on oxide ceramics: (a) react an oxygen active metal on the surface at high temperatures (active-metal metallizing) (b) fuse a glass-metal composite to the ceramic surface (dispersion metallizing). Both of these techniques require high temperatures to allow chemical reaction and diffusion to take place between the metallizing layer and the ceramic surface. These techniques also allow irregular penetration of the metallizing into the ceramic, particularly in the polycrystalline ceramics having a high glass content in the grain boundaries.

11656

Mattox, D.M. and Kominiak, G.J. (Sandia Labs., Albuquerque, NM)
PHYSICAL PROERTIES OF THICK SPUTTER-DEPOSITED GLASS FILMS. J. of the Electrochem. Soc.: Solid-State Sci. and Technol. 120, no. 11, 1535-39, Nov. 1973

The coefficient of thermal expansion of 5μ thick rf sputter-deposited Corning 1720 glass films was measured using a centilever beam technique. The films were rf-bias sputtered in an argon and an argon-5% oxygen ($Ar/0_2$ films) gas mixture. It is suggested that the structural changes that occur in some glass films at temperatures far below the strain point of the bulk glass (670°C) are due to a combination of intrinsic stress and a high concentration of defects. Surface coverage by the sputter-deposited glass films is discussed.

11657

U.S. Navy Electronics Lab. Center, San Diego, CA)
NELC DESIGNERS GUIDE FOR LSI - VOL I. Rept. no. NELC/TD 263, 566 pp., June 30, 1973. AD 769 663. N00123-73-1772

This report presents guidelines and recommendations for the use of large-scale integrated circuits in new designs. The material presented is based on a detailed survey of the state of the art of microelectronic devices and the experiences of government and commercial users of these devices. The guide presents information on the following topics relating to LSI: design applications, process technologies, electrical characteristics, packaging considerations, availability of LSI circuits, design compatibility, reliability and handling precautions. This document will be updated periodically.

11661

Thomas, E.F. and Anstead, R.J. (NASA, Goddard SFC, Quality Assurance Div., Greenbelt, MD)
THE DEGRADATION CHARACTERISTICS AND MECHANISMS OF AN OPTICALLY COUPLED ISOLATOR. Rept. no. FMR 743.90-001, 50 pp., July 28, 1975

Optically coupled isolators were operated at room ambient temperatures with various constant dc currents applied to the light emitting diode for 3,500 hours. Half the devices received photodiode biasing and half received phototransistor biasing. Devices operated at full rated LED I_f exhibted a normal degradation; in the OCI "On" state I_{cc} equaled 26% for photodiode operation. Operation at 50% ratsd I_f resulted in far lesser degradation of I_{cc} for both types of biased devices.

11662

RCA
RCA COS/MOS TECHNOLOGY. 75 pp., 1973

This journal consists of various articles by RCA engineers and scientists encompassing the history of development of the COS/MOS technology and its advantages and various applications in industry.

11663

Weisberg, H. (RCA, Solid-State Div., COS/MOS IC and Liquid Crystal Operations, Somerville, NJ)
MOS--AN RCA PIONEERED TECHNOLOGY; COS/MOS--RCA'S THRUST IN DIGITAL LOGIC. pp. 3-5, Sept. 25, 1972

This paper reviews the development of COS/MOS logic circuits and projects, with some of the extensions of these circuits through 1975.

11665

Heuner, R. (RCA, Solid-State Div., MOS Circuit Design and Appl., Somerville, NJ)
COS/MOS STANDARD-PARTS LINE COMES OF AGE. pp. 12-17, Oct. 6, 1972

A major advantage of COS/MOS is the ability of the circuit to perform well in single gates and flip-flops as well as in complex MSI and LSI configurations. Much information is available on the unique characteristics and advantages of COS/MOS circuit configuration. This paper illustrates the broad foundation of COS/MOS standard parts and explains why COS/MOS is the correct circuit configuration for such a broad-based line of parts.

11666

Funk, R.E. (RCA, Solid State Div., MS Appl., Somerville, NJ)
COS/MOS SIMPLIFIES EQUIPMENT DESIGN. pp. 18-23, Oct. 5, 1972

Five characteristics of COS/MOS are of major importance to the logic-system designer: current-drain and power-consumption; input characteristics, switching-transfer performance; output characteristics; and switching-speed. These characteristics are discussed in detail. Specific values and ranges are given; value variations with temperature, power supply, and capacitive loading are also given. The broad range of system-applicable COS/MOS characteristics is illustratetd with reference to quantitative data gathered on a random selection of COS/MOS NAND gates from a variety of manufacturing lots. The quantities given are not necessarily the data-book minimum/maximum limits for NAND-gates, but they do represent the COS/MOS product line.

11667

Carley, D.R. (RCA, Solid-State Div., MOS IC & Liquid Crystal Eng., Somerville, NJ)
COS/MOS CIRCUITS FOR CONSUMER APPLICATIONS. pp. 29-32, Sept. 11, 1972

This paper describes the development of low-power digital integrated circuits for consumer applications. Several applications are described, including timekeeping applications (watches and clocks), digital tuning techniques for FM and television, and pocket pagers. The main technology discussed is complementary-symmetry MOS.

11668

Eaton, S.S., Jr. (RCA, Solid-State Div., COS/MOS Custom Circuit Design, Somerville, NJ)
TIMEKEEPING REVOLUTION THROUGH COS/MOS TECHNOLOGY. pp. 33-41, Sept. 25, 1972

In today's fast-moving society, applications for timekeeping devices seem almost endless. Modern wristwatches and clocks have become indispensible items, and housewives enjoy the conveniences of oven, washing-machine, and blender timers. Farmers rely on automatic sprinkling and feeding systems, photographers on exposure timers, and the military on timers for modern weapons. At present, most of these applications employ some form of mechanical timing element. The development of COS/MOS integrated circuits and their usefulness in electronic timing circuits promise to revolutionize the timing industry. The reasons are made clear in the discussions of various COS/MOS timing circuits and systems provided in this paper.

11669

Waas, G.J. (RCA, Solid-State Div., MOS IC Circuit Design, Somerville, NJ)
DOING YOUR OWN THING. COS/MOS CUSTOM DESIGN. pp. 42-44, Oct. 4, 1972

There comes a time in the course of a product design when the engineer must choose between designing-in a custom circuit or fabricating with off-the-shelf standard parts. This is not a trivial decision. The reasons for choosing COS/MOS as the circuit technology are adequately covered elsewhere; it suffices to say that COS/MOS offers the high packing density of MOS with logic speeds approaching that of TTL. It is this high packing density and low power that often makes COS/MOS a candidate for custom designs. This article delineates some of the reasons for choosing either a standard circuit or custom approach and briefly discusses the steps necessary to move from a design concept to a finished custom device. An understanding of the capabilities and limitations of COS/MOS circuit development is necessary to exploit the full potential of custom design.

11670

Morgan, D.K. (RCA, Solid-State Div., COS/MOS Integrated Circuit Design, Somerville, NJ)
COS/MOS INTEGRATED CIRCUITS IN THE AUTOMOBILE ENVIRONMENT. pp. 45-51, Sept. 18, 1972

A variety of functions required in typical automobile systems can be readily implemented by COS/MOS monolithic integrated-circuit technology. The main emphasis of this paper, however, is placed on system approaches to the use of COS/MOS integrated circuits with light-emitting diodes. Incandescent display devices (Numitrons), and liquid crystals in digital-display automobile clock systems.

11671

Heuner, R.C. (RCA, Solid-State Div., MOS Circuit Design and Appl., Somerville, NJ)
LIQUID CRYSTALS AND COS/MOS OFFER MINIMAL POWER DIGITAL DISPLAYS. pp. 52-5, Sept. 20, 1972

Liquid crystals driven by complementary symmetry, metal-oxide-semiconductor integrated circuits offer the potential for low-cost, minimal-dissipation, digital display systems. An understanding of the capabilities and limitations of the liquid-crystal and COS/MOS technologies is necessary to successfully realize that potential. Interface requirements and drive circuitry, including implemented multiplexing techniques, are discussed; sample applications are outlined.

11672

Litus, J., Jr. (RCA, Solid-State Div., MOS IC Design Automation, Somerville, NJ)
KEEPING UP WITH THE TIMES THROUGH COMPUTER-AIDED DESIGN. pp. 56-61, Sept. 17, 1972

Computer-aided design allows quick realization of new designs and produces efficient and error-free designs at low cost. This paper discusses computer-aided design--specifically artwork generation, simulation, and testing--as presently practiced in the Solid State Div. in the design of COS/MOS integrated circuits.

11673

Vincoff, M.N. (RCA, Solid State Div., COS/MOS Appl. Eng., Somerville, NJ) and Schnable, G.L. (RCA, Res. Lab., Process and Appl. Matls., Princeton, NJ)
COS/MOS IS A HIGH-RELIABILITY TECHNOLOGY pp. 62-68, Oct. 18, 1972

This paper describes the manufacturing steps and the reliability features of the COS/MOS product lines. The various, constantly updated, quality-conformance criteria, including Groups A,B, and C testing,that assure control of the entire produce series are discussed. The high-reliability programs of MIL-STD-883 screening tests and the new quality and testing constraints of MIL-M-38510 are also covered, as are the failure mechanisms of MOS devices and reliability advantages of COS/MOS devices. Calculated reliability figures of failure rate and MTTF for COS/MOS devices are presented along with histograms on thousands of hours of operating life tests covering significant parameters.

11674

Morgan, D.K. and Steudel, G. (RCA, Solid-State Div., COS/MOS Integrated Circuit Design, Somerville, NJ)
COS/MOS PHASE-LOCKED-LOOP -- A VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS. pp. 69-75, Sept. 11, 1972

Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. Signal conditioning, FM demodulation, FSK demodulation, tone decoding frequency multiplication, clock synchronization, and frequency synthesis are some of the many applications of a PPL. The PLL described in this paper is the COS/MOS CD4046A, which consumes only 600 W of power at 10 kHz; a reduction in power consumption of 160 times when compared to the 100 mW required by similar monolithic bipolar PLL's. This paper discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

11675

Ruiz, H.J., Williams, C.S. and Padovani, F.A. (Tex. Instr. Inc., Dallas, TX)
SILICON SLICE ANALYZER USING A He-Ne LASER. J. of the Electrochem. Soc. 121, no. 5, 689-92, May 1974

Design criteria and performance characteristics are presented of an optical system capable of detecting imperfections (fractures, scratches etc.) on the polished surfaces of semiconductor materials. This instrument is also capable of providing fast and accurate defect counting and distribution on polished, etched semiconductor surfaces. The principle involved is that of scanning a He-Ne laser which is focused on the surface of the slice and analyzing the reflected and scattered light via polarizers and photomultipliers.

11676

Mo, R.S. and Gilbert, D.M. (Xerox Corp., El Segundo, CA)
RELIABILITY OF NiCr "FUSIBLE LINK" USED IN PROM's. J. of the Electrochem. Soc.: Solid-State Sci. and Technol. 120, no. 7, 1091-03, July 1973

It is shown here that the fuse failure times for a given stress obey the Weibull distribution, and the failure times are temperature dependent, obeying the Arrhenius equation. Excepting for certain grossly abnormal fuse runs, the unblown fuse life is generally adequate though by no means negligible, for a 1024 bit PROM. For the blown fuses, healing can occur. No heal model is available yet. However, it is established that the heal problem can be greatly reduced if proper blowing conditions as well as circuit biasing and sensing conditions are achieved.

11677

Olson, H.C. and Knauss, G.L. (Sandia Labs., Hybrid Eng. Div., Albuquerque, NM)
RF HYBRID MICROCIRCUIT SOLDERING TECHNIQUES. Rept. no. SLA 73-1073, 42 pp., Aug. 1974

The radar group at Sandia Laboratories, Albuquerque, has incorporated hybrid microcircuit technology in their new development effort. To minimize the inductance caused by "flying wires" it was desirable to attach most applique parts to the hybrid circuits using a solder alloy. The hybrid circuits have 60 KÅ of gold as the metallization to which the applique parts are attached. This report describes the solder development activities, equipment and assembly techniques using a 50%, by weight, lead-indium solder alloy.

11678

Canepa, R. (U.S. Army, Electronic Command, Fort Monmouth, NJ)
NUCLEAR RADIATION EFFECTS ON THE RCA GUA-5 (ECOM LSI RADIAC COUNTER CIRCUIT). Rept. no. ECOM-4352, 20 pp., Sept. 1975

Operational pulsed reactor and linear accelerator (LINAC) exposure of the counter section of the large scale integrated (LSI) radiac circuit were conducted at the White Sands Missile Range. The LSI was fabricated at ECOM, and was based on the RCA Universal Gate Array. The counter was driven externally. The effects of neutron fluence which causes circuit damage and the gamma dose which causes the circuit to miscount as well as transient upset, were investigated.

11679

Killiany, J.M., Saks, N.S., Baker, W.D. et al. (U.S. Navy, Naval Res. Lab., Washington, D.C.)
EFFECTS OF RADIATION ON BURIED-CHANNEL CCDs WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION. Appl. Phys. Letters 24, no. 10, 506-08, May 15, 1974

The effects of gamma radiation on the operation of a buried-channel charge-coupled device having doped polysilicon electrodes and undoped polysilicon interelectrode isolation were studied. Doses up to 1×10^4 rad caused no increase in the transfer inefficiency. At a dose of 3×10^4 rad, the flat-band voltage shift was sufficient to drive the buried channel out of depletion and to cause field-induced channeling in the undoped polysilicon isolation regions. Increasing the channel bias returned the channel to depletion. However, channeling of the isolation regions could not be eliminated by changing the clock and bias voltages.

11680

Buehler, M.G. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Washington, D.C.)
THERMALLY STIMULATED MEASUREMENTS: THE CHARACTERIZATION OF DEFECTS IN SILICON p-n JUNCTIONS. pp. 549-60, 1973. F19628-71-C-0912

Thermally stimulated capacitance and current measurements utilize the ability of defects in the vicinity of a p-n junction to trap holes or electrons and to emit them after receiving sufficient thermal energy. Values for defect densities, energy levels, and emission rates can be derived from these measurements where the limit of detectability can be as low as 10^{10} defects/cm^3. From these values the atomic nature of the defects can be identified.

11681

Lipman, J.A. (Tex. Instr. Inc., Semiconductor Group, Dallas, TX)
REWORK OF LINEAR INTEGRATED CIRCUITS. Rept. no. AFWL-TR-74-53, May 23, 1972-Feb. 18, 1974, 72 pp., June 1974. AD 786 024. F29601-72-C-0095

A-C probe technique and controls were evaluated to ensure radiation hardness of integrated circuits. A dielectrically isolated, photocurrent compensated linear IC was the test vehicle. A special metal pattern was used to isolate and provide probe pad leads for each active device on the IC. Air Force Weapons Laboratory personnel then probed the devices to determine the parameters that might indicate neutron hardness assurance. After the probing, the metal pattern was removed from a number of the devices which were then processed normally with NiCr, metal and quartz overcoat. Possible damage to the silicon transistors caused by the special or the normal processes was evaluated by photographing a number of the bars and some slices from the devices. A unique procedure was used to label the separate bars so that their physical location on the slice could be determined after dicing.

11682

Adams, J.R. (Sandia Labs., Albuquerque, NM) and Bonham, H.B. (Bendix Corp., Kansas City, MO)
ANALYSIS AND DEVELOPMENT OF A THERMO-COMPRESSION BOND SCHEDULE FOR BEAM LEAD DEVICES. IEEE Trans. on Parts, Hybrids, and Packaing PHP-8, no. 3, 22-6, Sept. 1972

This paper discusses the practical considerations of beam lead wobble tool bonding, and describes the theoretical and experimental techniques which were used to establish the critical bonding variables. Using these techniques a bond schedule has been developed in terms of only two variables, bond force and interface temperature.

11683

Margraff, T.C. (U.S. Air Force, Wright-Patterson AFB, Air Force Inst. of Technol., OH)
DESIGN AND PERFORMANCE OF A CCD MEMORY SYSTEM. Rept. no. GE/EE/74-56, 82 pp., Dec. 1974. AD/A008 657

Three charge-coupled devices, the Fairchild 9216, the Fairchild LARAM, and the Bell Northern CC8M01 are analyzed to determine their suitability as components in a memory system. After comparing access time, configuration flexibility, and power consumption, the LARAM is chosen as the primary storage component for the mass memory unit. A memory system whose primary purpose is to test the operation of the CCD's is designed. The system has a capacity of up to ten LARAM devices. Various refresh intervalperiods and two operating frequencies, 5 MHz for refresh and 1.25 MHz for read/write operations are provided. Operational control of the system is provided through the console of the Hewlett Packard 9820A programmable calculator. To facilitate testing, the calculator provides a record of all address locations and data words used.

11684

Cook, H.B. (U.S. Army Missle Command, U.S. Army Missile Res., Dev. and Eng. Lab., Redstone Arsenal, AL)
HIGH POWER PULSE TESTING OF INTEGRATED CIRCUITS. Rept. no. RG-72-22, Tech. Rept., 60 pp., Dec. 5, 1972. AD 755 807

The objective of this work was to augment the component high power pulse damage work. The failure modes and mechanisms were investigated for integrated circuits when various pin pair combinations were stressed with high power pulses Attempts were made to correlate the parameters of the high power pulse to the time before secondary breakdown. Pre- and post-test voltage-current measurements were taken on the pin pair combinations to determine if damage had occurred. Failure analysis were performed on selected integrated circuits to determine the failure mechanisms. The predominant failure mechanism observed was flashover with associated metallization melting and alloying. Due to the complicated geometries of the integrated circuits, no correlation was evident between the time before secondary breakdown and any of the measured pulse parameters.

11685

Jurison, J. (Rockwell Internatl. Corp., Autonetics Div., Anaheim, CA)
MOS/LSI FOR AEROSPACE COMPUTERS: PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS. Rept. no. X72-73/401, 13 pp., Dec. 20, 1971. AD 900 572L. IDEP Acc. no. D7381. IDEP 347/00.00.00.C1.52

In total this company has accumulated over 5.5 million device hours under different test conditions with excellent results. This paper presents the results of these reliability tests, placing particular emphasis on quantative data rather than generalizations. The data are also being compared with earlier estimates made using a reliability transfer model developed from bipolar failure mode analysis. In addition, reliability growth projections are shown together with predictions of future spacecraft computer reliabilities for extended space missions.

11687

Anon.
PROCEEDINGS OF THE TECHNICAL PROGRAM. 1975 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE. 284 pp., Anaheim, CA., Feb. 11-13, 1975, New York, NY June 17-19, 1975

Sessions:

I Electrodeposits for PC Board Tips
II Soldering Materials and Solderability
III Photochemical Machining
IV PWB Materials Problems
V ATE Systems -- New Developments and Trends
VI Application of Solder and Soldering Techniques Associated with the Electronic Industry
VII Software Packages for Logic-Circuit Testers

CONNECTOR SYMPOSIUM

I Military/Aerospace/Oceanographic Connector Applications
II Commercial & Industrial Connector Applications
III Offsetting the High Cost of Gold

11688

Gluntz, G.H. (E. I. du Pont de Nemours & Co., Inc., Berg Electronics Div., New Cumberland, PA)
LOW PROFILE DOUBLE BEAM IC SOCKET. pp. 259-61. 1975 NEPCON Proceedings

In 1972, our company, in conjunction with the Burroughs Corporation, developed a family of dual-in-line sockets. This connector family provides a means of opposing the rising costs of servicing electronic business machines by facilitating the repair of cards in the field, rather than replacement of the cards.

11689

Anon.
PROCEEDINGS 1975 ANNUAL RELIABILITY AND MAINTAINABILITY SYMPOSIUM. Cosponsored by IEEE Reliability Group, IES, ASME Aerospace Div., ASQC Reliability Div. and Electronics Div., AIAA System Effectiveness and Safety Technical Committee, AIIE and SOLE. Washington, D.C. 606 pp., Jan. 28-30, 1975. IEEE Cat. no. 75 CHO 918-3 RQC

Sessions:

1A Assurance Technology Payoffs
1B Nuclear Systems Safety
1C Maintainability Technology
1D 1975 System Effectiveness Task Status Report
2A Life Cycle Cost (LCC) Analysis--Case Studies
2B Reliability Testing and Evaluation
2C Electronic Controls for Aircraft Engines
2D Human Performance Reliability Modeling
3A Quality and Reliability on the International Scene
4A Logistics Interfaces with R&M
4B Nuclear Systems Reliability
4C Math Modeling
4D Maintainability Engineering/Field Data
5B Operation and Support Cost
5C Direct Method in Sequential Analysis
5D Some Recent Developments in Reliability Demonstration
6A Reliability of Major Mechanical Systems
6B Paper Fair
6C Techniques and Approaches to IC Testing
6D AWACS--Application of System Assurance Technology
7A Contracting and Management
7B Army RAM Payoffs
7C Power Systems Reliability -- R
7D Introduction to Software Reliability
8A Reliability to Mechanical Parts and Subsystems
8B Hazards Analysis
8C Modeling for Measures of Effectiveness

11690

Kline, A.J. and Kermode, A.W. (JPL, Calif. Inst. of Technol., Pasadena, CA)
DEVELOPMENT OF BEAM LEAD RF INTEGRATED CIRCUITS. pp. 349-53. NAS7-100. 1975 Annual Reliability and Maintainability Symposium

This paper describes the design and development of a set of multifunction VHF/UHF integrated circuits aimed at providing a major improvement in spacecraft radio reliability through low stress operation and the processing of these circuits in beam-lead form. The methods evolved for the high frequency characterization of the devices are discussed together with the design of suitable test fixtures. Typical test results and the distribution of test parameters are presented. A unique carrier for beam-lead devices is described, and the need for such a device is discussed. Initial probe tests of the devices, done by conventional means, are correlated to the detailed UHF tests. The application of the carrier to device screening, burn-in and drift measurements is discussed together with the incentives for providing these capabilities. An overview of the integration of the devices into the spacecraft radio is given and candidate assembly processes are discussed. The technology impact of this approach upon future spacecraft radio systems is qualitatively examined.

11691

Burns, D.J. and Kapfer, V.C. (U.S. Air Force, RADC, Griffiss AFB, NY)
A COMPARATIVE RELIABILITY EVALUATION OF C/MOS: A MATURING TECHNOLOGY. pp. 354-59. 1975 Annual Reliability and Maintainability Symposium

A reliability evaluation program consisting of 180 C/MOS devices from 4 vendors has been in progress at RADC for about 2 years. The date codes for these devices range from 1969 to 1973. The testing program included storage temperature, thermal shock, moisture resistance w/bias, temperature cycling w/bias. and bias power and temperature step stress (BPATSS). The results are presented detailing the predominant failure modes and mechanisms which were induced by this stress testing program.

11692

Adams, T.P. (GE Med. Systems, Milwaukee, WI) and Fasano, M.D., Jr. (GE, Valley Forge SC, Philadelphia, PA)
THE MICROCIRCUIT PACEMAKER SPACE AGE SPIN-OFF TO ACHIEVE RELIABILITY AND LONG LIFE. pp. 360-65. 1975 Annual Reliability and Maintainability Symposium

The paper will specifically address the importance of miniaturization and high reliability to the success of pacemaker operation, the general theory of operation, comparisons of discrete devices and hybrid microcircuits, design concepts, description of configurations and circuitry, procurement policies and principles, processes utilized, assembly and inspection procedures and testing philosophies.

11693

Derr, J.H., Van Hoorde, G.R. and Girdis, J.J. (Ford Motor Co., Dearborn, MI)
PREDICTING THE RELIABILITY OF SYSTEMS USING COMPLEX MOS/LSI DEVICES IN AUTOMOTIVE APPLICATION. pp. 366-71. 1975 Annual Reliability and Maintainability Symposium

This paper presents a prediction model for MOS/LSI devices when exposed to automotive environments, assuming that proper design concepts have been employed to protect the devices from the mechanical stresses, electrical environment and other unusual conditions present. The model is based upon empirical documentation from various sources and is aimed primarily at ceramic, non-beam leaded LSI devices. The logic steps involved in the present paper are:

1. Presentation of an LSI mathematical model
2. Development of active mission time and dormancy factors
3. Development of environmental multipliers
4. Development of quality screening multipliers

11694

Homan, R.A. and Rossman, M.W. (Martin Marietta Corp., Denver, CO)
EVALUATION TESTING OF INTEGRATED CIRCUITS. pp. 372-76. 1975 Annual Reliability and Maintainability Symposium

Evaluation/qualification test approaches applied to various types of integrated circuits are summarized. Linear devices as well as C-MOS and TTL digitals were evaluated. Among the evaluation techniques utilized were computerized circuit modeling and simulation for purposes of nominal, worst case, and sensitivity analyses, physical construction analysis, node voltage probing on both digital and linear devices, characterization by means of exploratory and design limit testing. Other tests performed were environmental, burn-in, life, specification limit, and functional tests. The data analysis approach, typical results and observations on the effectiveness of the various techniques are presented.

11695

Reich, B. (U.S. Army, ECOM, Fort Monmouth, NJ)
MILITARY IC STANDARDIZATION, ACQUISITION AND TECHNOLOGY. pp. 404-07. 1975 Annual Reliability and Maintainability Symposium

This paper presents the findings and recommendations of the JLC's Ad Hoc Group on Managerial Aspects of Electronic Equipment Reliability and the progress made in implementing its recommendations by its successor, the Joint Technical Coordinating Group on Electronic Equipment Reliability (JTCG). The prime emphasis of both groups was in the area of integrated circuits, often called microcircuits, and concerned with the feasibility of taking effective management actions relative to the procurement of low cost, reliable electronic equipment.

11696

Fresh, D.L. (Aerospace Corp., El Segundo, CA)
RELIABILITY ON INTERCONNECTIONS ON MICROCIRCUITS. pp. 568-72. 1975 Annual Reliability and Maintainability Symposium
Rept. no. SAMSO-TR-75-92,
Rept. no. TR-0075(5901-02)-4, 5 pp.,
F04701-74-C-0075

Defects in metal interconnection patterns constitute a significant factor in the reliability of semiconductor microcircuits. Electrical opens, occurring in the vacuum-deposited metal films, have been the basis for reliability studies by numerous investigators. The application of the scanning electron microscope (SEM) is becoming relatively widespread in detecting these defects in metallization. Considerable work has recently been directed toward improvement of the SEM procedures and techniques, including the preparation of a test method in MIL-STD format. The current status of the SEM test method; its utility, suitability, and acceptance in detecting defects in metal interconnection patterns; and its extension and applicability to other types of defects in high reliability semiconductor microcircuits are discussed.

11697

Guidici, D.C. (Fairchild Semiconductor, Mountain View, CA)
RIBBON WIRE VERSUS ROUND WIRE RELIABILITY FOR HYBRID MICROCIRCUITS. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 2, 159-63, June 1975

In an effort to create a more reliable bond interface in hybrid microcircuits, a study was launched to evaluate the relative bond strengths of round wire and ribbon wire of comparable cross section, and to determine which is inherently more reliable after thermal degradation. This paper presents a comparative bonding reliability study of aluminum ribbon wire versus round wire, and gold ribbon wire versus round wire in hybrid microcircuits. The wires are ultrasonically bonded to thick film gold, thin film aluminum, thin film chromium-gold, and thin film molybdenum-gold. Results showed that ribbon wire was superior to round wire and, that after 1000 hours of high temperature storage, aluminum round wire averaged 91% bond degradation on all types of substrates, while gold ribbon wire averaged 57% degradation.

11698

Hall, P.M. Panousis, N.T. and Menzel, P.R.(Bell Telephone Labs., Inc., Allentown, PA)
STRENGTH OF GOLD-PLATED COPPER LEAD ON THIN FILM CIRCUITS UNDER ACCELERATED AGING. pp. 133-36. Proceedings 1975, 25th Electronic Components Conference. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 3, 202-05, Sept. 1975

The strengths of thermocompression bonds made between gold plated copper lead frames and gold metallized thin film circuits decreased in time when aged at 200-300°C in air or vacuum unless there is a diffusion barrier (such as nickel) between the copper and gold. After pulling bonds to destruction, failure modes and failed surfaces were characterized by scanning electron microscopy, Auger spectroscopy, electron microprobe, stylus probe, and x-ray diffraction. The failed surface on the bond was very rough, appearing to consist of mountains of almost pure Cu resting on a relatively smooth layer of grains, identified as Cu_3Au, where the Cu_3Au regions were visible in the valleys between the copper mountains. The mating failed surface on the lead side of the bond was similarly rough, but with only a few scattered grains of Cu_3Au evidently pulled out from the opposite surface.

11699

Cohen, S. (RCA Corp., Solid State Div., Somerville, NJ)
TOTAL-DOSE RADIATION-HARDENED COS/MOS INTEGRATED CIRCUITS. Rept. no. PRRL-75-CR-16, Ann. Rept., Oct. 8, 1973-Dec. 31, 1974, 29 pp., Mar. 14, 1975. AD/A 007 618. N00014-74-C-0079

The work on radiation hardened COS/MOS integrated circuits described in this report was done in two phases. Under Phase I we sought to evaluate the effects of various SiO_2 channel-oxidation techniques on the radiation susceptibility of bulk-silicon and SOS COS/MOS circuits. We also prepared procedures for ion-implanting of aluminum in channel oxide and for evaluating characteristics that could be used to predict the radiation hardness of processed wafers. Under Phase II, emphasis has been placed on developing techniques for improving the radiation hardness of COS/MOS circuits on sapphire substrates, and radiation-hardened COS/MOS on bulk silicon integrated circuits were produced.

11700

Antler, M. (Bell Labs., Columbus, OH)
GOLD CONNECTOR CONTACTS: DEVELOPMENTS IN THE SEARCH FOR ALTERNATE MATERIALS. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 3, 216-20, Sept. 1975

The characteristics of electroplated and wrought gold-based contact materials for high reliability connectors in low energy circuit applications are reviewed. To insure that contacts do not degrade by film formation due to corrosion, diffusion, or wear processes, certain practices have evolved on the compositions, thicknesses, porosities, hardness and manufacturing methods for the golds, and for underplatings that are used with them. Recently, however, its escalating cost has stimulated intensive work which shows that the thickness of gold required for satisfactory performance can often be reduced. In addition, manufacturing techniques which selectively locate gold to the mating area of a contact have come into vogue. Other routes to cost reduction include the use of nonnoble materials, palladium, or golds alloyed with large amounts of base metals.

11701

Lyman, J.
SPECIAL REPORT: FILM CARRIERS STAR IN HIGH-VOLUME IC PRODUCTION. Electronics 48, no. 26, 61-68, Dec. 25, 1975

The film in present film carriers preserves the configuration of the fragile copper IC interconnect or spider and acts as an insulator. But its presence adds to the final cost of the IC. In addition, many plastics contain metallic ions that could contaminate an adjacent chip. For these reasons, several companies are now experimenting with etching IC patterns on copper foil unsupported by plastic film. There are a couple of drawbacks, though. As Thomas Angelucci, president of International Micro Industries, points out, "An all-copper system will not be possible to test in process--say, at the point where all inner bonds are made and the semifinished ICs are reeled up. Only an insulated tape is capable of this. Also, present-day machines are designed to run with plastic films, not copper foil so considerable machine redesign may be needed."

11702

Lau, S.S., Mayer, J.W., Nakamura, K. et al. (Calif. Inst. of Technol., Div. of Eng. and Appl. Sci., Pasadena, CA)
ANALYSIS OF SEMICONDUCTOR STRUCTURES BY NUCLEAR AND ELECTRICAL TECHNIQUES. Rept. no. AFCRL-TR-0550, Sci. Rept. no. 2, 43 pp., Oct. 15, 1975. F19628-75-C-0008

In this report we present three studies of thin film reactions between metal films and Si. In these studies we have MeV He ion backscattering spectrometry, Auger electron spectroscopy, secondary electron microscopy and glancing angle x-ray diffraction as the principal tools of analysis. 1. At temperatures well below the Si-Al eutectic (577°C), fine grained polycrystalline Si (poly Si) in contact with Al films recrystallizes in the Al matrix. The recrystallization can be deferred or suppressed by placing a buffer layer of V or Ti between and Al film and poly Si. 2. When annealing Pt films deposited on Si in an O_2 ambient the formation of PtSi does not consume all the Pt. The top layer of Pt is separated from the underlying PtSi by a thin SiO_2 layer. 3. The formation of Ni silicide depends on the structural characteristics of the Si substrate. The growth of the silicide (Ni_2Si) initially formed is faster on <100> and poly Si than on <111> Si. For Ni on amorphous Si, NiSi also appears.

11703

Zimmerman, T.A., Miller, C.S. et al. (TRW Systems Group, Redondo Beach, CA)
CHARGE COUPLED DEVICES IN SIGNAL PROCESSING SYSTEMS VOL. II. ANALOG SIGNAL PROCESSING. 85 pp., Dec. 1974. AD/A011 499. N00014-74-C-0068

The application of CCD's to analog signal processing was investigated. The ideal analog application of CCD's is the correlation function. Both recursive and nonrecursive analog sampled data filters are discussed. CCD matched filter designs are analyzed and design criteria derived. System applications and detailed. These include range gated filters, doppler comb filters, and IFF beacons for radar systems; analog recursive filters and correlators for communication systems; and memories for processing systems.

11704

Kirk, W.J., Jr., Carter, L.S. and Waddell, M.L. (Bendix Corp., Kansas City Div., Kansas City, MO)
CONTROL OF ELECTROSTATIC DAMAGE TO SOLID STATE DEVICES. Rept. no. BDX-613-1080, Technol. Spinoff Rept., 24 pp., Mar. 1974. N75-10830. AT(29-1)-613 USAEC

Static voltages generated on human bodies by normal movement of assembly personnel can degrade or destroy many solid state devices not normally expected to be susceptible to damage from such a source. An energy-storage model of the human body was developed and used to determine the levels of static voltage that degrade various devices. A system was assembled and used to continuously monitor and display the level of static voltage on an operator. The additional problem of static voltages created by solvent-spraying was studied and the benefits of varying the solvent volume resistivity were verified.

11706

Schanable, G.L., Kern, W., and Comizzoli, R.B. (RCA Labs., Princeton, NJ)
PASSIVATION COATINGS ON SILICON DEVICES. J. of Electrochem. Soc.: Solid-State Sci. Technol. 122, no. 8, 1092-1103, Aug. 1975

This paper reviews the materials and techniques used to apply passivation coatings to completed silicon devices. Principal production techniques used in passivation of silicon devices include thermal oxidation, high-temperature diffusion, high-temperature chemical vapor deposition of Si_3N_4 or Al_2O_3, low temperature chemical vapor deposition of glass-like SiO_2 or phosphosilicate layers (deposited at approximately 400°C), rf sputtering of SiO_2 mechanical deposition of glass frit layers which are subsequently fused, and application of organic polymer films. The effects of passivation layers on silicon device reliability are discussed, and the interrelationships among the silicon device, the passivation layer or layers used and the final encapsulation are indicated.

11707

Dickson, F.H. and Garrett, J.C. (Collins Radio Co., Dallas, TX)
PACKET RADIO COMMUNICATIONS COLLINS RADIO COMPANY. Rept. no. 523-0699923-001C3L, Quart. Tech. Rept., Oct. 1, 1973-Sept. 30, 1975, 38 pp., Mar. 31, 1975. AD/B003 570L. DAHC15-73-C-0192

This project has focused on the impact of rf channel, network design, and technology on the repeater because it is the critical communications element in a packet radio network. It can be converted to a station by adding a minicomputer, and to a terminal by adding appropriate I/O components. Since a repeater has been successfully implemented, it is reasonable to conclude that a packet radio network is technically feasible. Future experiments must be aimed at demonstrating operation of an entire network.

11708

Dunkley, J.L., Bayazit, Y.N. and Tickle, A.C. (Solid State Res. Corp., Scottsdale, AZ)
INTEGRATED DEVICE ANALYSIS MODELING AND DESIGN. Rept. no. AFAL-TR-75-169, Final Tech. Rept., Feb. 1, 1973-Jan. 1, 1975, 258 pp., Sept. 1975. F33615-73-C-1161

This report presents results of a study of a multi-section, two dimensional non-linear transistor and resistor model amenable to computer analysis for significantly improved circuit analysis compatible with SEPTRE, TRAC, and TIME. Theoretical considerations were primarily developed by the staff of Solid-State Research Corporation.

11709

Eisen, F.H., Higgins, J.A. and Immorlica, A.A. et al. (Rockwell Internatl. Sci. Center, Thousand Oaks, CA)
INVESTIGATION OF THECNOLOGICAL PROBLEMS IN GaAs. Rept. no. AFCRL-TR-75-0435, Rept. no. SC5017.4SAR, Semiann. Tech. Rept. no. 1, 116 pp., July 25, 1975

Various technological problems in the development of GaAs microwave devices are covered in this report. The goal is to advance the state-of-the-art in material and device technology. The work reported here includes epitaxial growth of high-resistivity and multiple ultrathin films, study of the relationship between device performance and material parameters using FETs and p-n junctions, study of noise and impact ionization coefficients in IMPATT structures under high electric field, preparation of high-quality oxide films for surface passivation, growth of semi-insulating substrates, and characterization techniques and study of ion implantation as a tool for microwave device fabrication. The activities and the progress made during the six-month period are described in separate sections. Future plans for the next reporting period are also included.

11710

Ham, W.E. (RCA Labs., Princeton, NJ)
HIGH SPEED COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR/SILICON-ON-SAPPHIRE. Rept. no. ERRL-75-CR-42, Final Rept., Phase II, Dec. 1, 1972-Apr. 30, 1975, 60 pp., Nov. 1975. N00014-73-C-0090

This study consisted primarily of two parts. The first part was a study of the physical structure of the edge region of silicon-on-sapphire islands. The second part of the study consisted of examining the electrical properties of the edge region, particularly after irradiation.

11711

Jellison, J.L. (Sandia Labs., Albuquerque, NM)
EFFECT OF SURFACE CONTAMINATION ON THE THERMOCOMPRESSION BONDABILITY OF GOLD. pp. 271-77. Proceedings 1975, 25th Electronic Components Conference. IEEE Trans. on Parts, Hybrids, and Packaging PHP-11, no. 3, 206-11, Sept. 1975

The recent development of a microshear test has made possible the quantitative study of the effect of surface contamination on thermocompression ball bonding of gold to gold metallization. Contaminant films were characterized by Auger electron spectroscopy and low energy ion spectroscopy. The thermocompression gold bonding process was found to be highly temperature dependent when organic films, which are barriers to metallic bonding, are present. Much of this temperature dependence could be eliminated by removing the contaminant films by uV radiation prior to thermocompression bonding. Post-heat treatment resulted in the growth of metallic bond interfaces, presumably by sintering mechanisms.

11712

Holloway, P.H. and Long, R.L. Jr., (Sandia Labs., Albuquerque, NM)
ON CHEMICAL CLEANING FOR THERMOCOMPRESSION BONDING. IEEE Trans. on Parts, Hybrids and Packaging PHP-11, no. 2, 83-88, June 1975

The removal of a Cr_2O_3 contaminant oxide film from gold surfaces by a ceric ammonium nitrate (CAN) etch and two different potassium iodide plus iodine (KI + I_2) etchants was investigated using Auger electron spectroscopy and thermocompression (TC) bonding. It was shown that CAN effectively attacked and removed the Cr_2O_3 while the KI + I_2 attacked the underlying gold film. The KI + I_2 improved the TC bondability both by undercutting some of the Cr_2O_3 and by roughening the gold, thereby allowing more deformation to occur during bonding. The implications of these results on selection of a chemical cleaning agent are discussed. The ability of CAN to dissolve a chromium adhesion layer under the gold metallization has also been investigated. It was shown that a heat treatment of 300°C for two hours in air prevented this undercutting; possible reasons are discussed.

11713

Satake, T. (Nippon Elec. Co., IC. Div., Kawasaki, Japan)
ELECTROMIGRATION FAILURE IN NiCr THIN-FILM STRIPES. Appl. Phys. Letters 23, no. 9, 496-98, Nov. 1, 1973

Electromigration-induced failure in NiCr thin film stripes is investigated. The composition of evaporated NiCr thin films is 77:23 Ni/Cr in weight %, according to a spectroscopic analysis. The mean time to failure of NiCr thin-film stripes can be qualitatively expressed by a relation similar to that held in the MTF of Al thin-film stripes, i.e., $MTF^{OC} J^{-n} \exp(\phi/kT)$. However, the values of n and ϕ of NiCr are 13 and 1.4 eV, respectively, whereas those of Al are 2 ~ 3 and 0.41 eV, respectively.

11714

Bube, K.R. and Hitch, T.T. (RCA Labs., Princeton, NJ)
BASIC ADHESION MECHANISMS IN THICK AND THIN FILMS. Rept. no. PRRL-75-CR-18, Quart. Tech. Rept. no. 1, Jan. 1-Mar. 31, 1975, 35 pp., Apr. 30, 1975.
N00019-75-C-0145

This second-year effort is directed to expanding the basic study to include silver and copper films as well as gold. By way of comparison, gold thick films are highly conductive, corrosion-resistant, thermo-compression bondable, virtually free from electrolytic migration, and compatible with ruthenium-based thick-film resistor systems and cross-over dielectric materials. However, gold films are readily dissolved by tin-bearing solders and thermally aged soldered joint strength is poor. Silver films are considerably less expensive, on an ounce-for-ounce basis, than gold and are not subject to severe electrolytic migration, if used in hermetically sealed packages. With silver films, however, special geometric and processing precautions must be exercised when silver is used as electrodes for Ru-based resistor systems. In addition, silver's high mobility in cross-over dielectric materials seriously limits its use in multilevel package designs. To successfully resist corrosion, silver films must be over coated or hermetically sealed. Copper thick films are also highly conductive and solderable, and represent the best low-cost alternative to noble metal films. Copper's limitations include the necessity to fire in a nitrogen or other inert atmosphere. Additionally, protection from moisture and corrosive ambients must be provided. Thermal aging characteristics after soldering are poor due to the formation and growth of copper-tin intermetallic compounds. Thermal aging characteristics after soldering are poor due to the formation and growth of copper-tin intermetallic compounds. A chief aim will be to identify relative microstructural effects on adhesion and thereby chart potentially different paths of improvement for gold, silver, and copper films. The basic study of microstructural effects upon adhesion will continue to be augmented by evaluation of processing upon commercial silver and copper inks.

11718

Anon.
14th ANNUAL PROCEEDINGS, RELIABILITY PHYSICS 1976. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. Caesars Palace, Las Vegas, NV., Apr. 20-22, 1976

Sessions:

Devices
Reliability Technology Basic Failure Analysis Techniques and Application
Applications of Surface Analytical Techniques to Failure Analysis
Bonding, Metallization and Hybrids
Printed Circuit Boards and Capacitors
PROMS
Encapsulation

11719

Thomas, E.F. (NASA, Goddard SFC, Greenbelt, MD)
THE MECHANISMS OF DEGRADATION IN AN OPTICALLY COUPLED ISOLATOR. 14th Annual Proceedings, Reliability Physics 1976

The degradation characteristics of an optically coupled isolator were defined for both photodiode and phototransistor operation. Although degradation was due mostly to degradation of the GaAs LED, additional degradation, due to channel formation within the transistor, was also observed. A discussion of the mechanisms causing the observed degradation is presented.

11720

Hewlett, F.W., Jr. and Pederson, R.A. (Bell Labs., Allentown, PA)
THE RELIABILITY OF INTEGRATED INJECTION LOGIC CIRCUITS FOR THE BELL SYSTEM. 14th Annual Proceedings, Reliability Physics 1976

The reliability of Integrated Injection Logic (I^2L) circuits fabricated in a standard bipolar technology with Au interconnection based on accelerated stress aging is reported. A threshold voltage for Au electrolysis has been identified. Successful operation of a nonisolated I^2L circuit without moisture protection in salt water has been demonstrated. This is possible because power supply voltage and logic swings are below the threshold of Au electrolysis. Bias temperature (20mW/300C) and bias humidity (24mW/85C/85% RH) stress of a 250-gate, T^2L-compatible, I^2L random logic chip indicate median lives of 600,000 and 100,000 hours, respectively, in these ambients for the main populations. Finally, step-stress data on I^2L current gain (Bu) from 150C to 325C under bias indicate only minimal degradation at higher temperatures. (The current gain must be 1.0 for logical operation).

11721

Potter, H.C. and Reber, D.R. (Bell Labs., Reading, PA)
A STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED, MONOLITHIC SILICON INTEGRATED CIRCUITS. 14th Annual Proceedings, Reliability Physics 1976

The transient and steady state characteristics of dielectric passivated SIC failure caused by charge spread on the dielectric surface has been studied. The results show that devices may recover after sufficiently long times under bias. The physical and electrical design characteristics leading to this effect are described.

11722

Abbas, S.A. and Davidson, E.E.(IBM, Hopewell Junction, NY)
RELIABILITY IMPLICATIONS OF HOT ELECTRON GENERATION AND PARASITIC BIPOLAR ACTION IN AN IGFET DEVICE. 14th Annual Proceedings, Reliability Physics 1976

For an IGFET whose channel is very short, the current gain of the lateral parasitic bipolar transistor that resides below the IFGET's surface can become significant. With sufficient drain voltage for impact ionization to occur, the bipolar region can conduct, causing the useful voltage range of the IGFET to be limited to a fraction of the drain breakdown voltage. Furthermore, the action of the bipolar region can lead to a profusion of hot electrons which, upon injection into the gate oxide, eventually cause a shift in threshold voltage, leading to device degradation and failure.

11723

Smith, J.S. and Talada, D.D. (U.S. Air Force, RADC, Griffiss AFB, NY)
A CMOS/SOS RELIABILITY STUDY. 14th Annual Proceedings, Reliability Physics 1976

This paper describes a program to evaluate the reliability of the CMOS silicon-on-sapphire (SOS) device technology. The program consisted of characterization, accelerated step stress testing and failure analysis of 160 CMOS/SOS circuits from three manufacturers. The significant failure mechanisms observed and their relationship to the SOS technology are described.

11724

Loro, A. (Bell Northern Res., Ottawa, Can.)
MICROSURGERY AS A TOOL IN THE ANALYSIS OF L.S.I. SILICON CHIPS. 14th Annual Proceedings, Reliability Physics 1976

The ability to open or bridge selected conductors on an L.S.I. chip opens up a wide range of analytical opportunities in the field of failure analysis, design debugging, mask error correction and competitive device analysis. Effective methods of severing, repairing and interconnecting conductors in high density L.S.I. silicon chips are described. The design criteria for a simple precision tool providing the dual functions of microsurgery and subsequent electrical probing of components are discussed. Results obtained with the methods described on various commercial and custom L.S.I. circuits are presented.

11725

Paulson, W.M. and Lorigan, R.P. (Motorola, Inc., Phoenix, AZ)
THE EFFECT OF IMPURITIES ON THE CORROSION OF ALUMINUM METALLIZATION. 14th Annual Proceeding, Reliability Physics 1976

Surface impurities are an important factor that affects the reliability of semiconductor devices exposed on THB environments. Aluminum metallized specimens were intentionally contaminated with controlled amounts of Na, K, and Cl. Corrosion was observed at both the anode and cathode following THB tests. A model is proposed to explain the observed corrosion processes.

11726

Hall, E.L., Koblinski, A. and Gragg, J. E., Jr. (Motorola, Inc., Phoenix, AZ)
BERYLLIUM -- A HIGH RELIABILITY THIN FILM METALLIZATION. 14th Annual Proceedings, Reliability Physics 1976

The use of pure beryllium-10wt% aluminum alloy as high reliability thin film metallizations on semiconductor devices is described. The important metallurgical properties, the processing, and the use on actual devices is discussed. Precautions for handling beryllium in a semiconductor processing environment are detailed since, in certain forms, it is a toxic material.

11727

Bushmire, D.W. (Sandia Labs., Albuquerque, NM)
GOLD ALUMINUM INTERMETALLICS ON THIN FILM HYBRID MICROCIRCUIT SUBSTRATES. 14th Annual Proceedings, Reliability Physics 1976

The effects of gold aluminum intermetallic growth on the reliability of interconnects to thin film hybrid microcircuits have been studied. The most reliable combinations of three different metallization systems and four different wire systems are determined.

11728

Newsome, J.L., Oswald, R.G. and Rodgriques De Miranda, W.R. (Honeywell, Inc., St. Petersburg, FL)
METALLURGICAL ASPECTS OF ALUMINUM WIRE BONDS TO GOLD METALLIZATION. 14th Annual Proceedings, Reliability Physics 1976

A study is made of the intermetallics which form when aluminum wire is ultrasonically joined to thin and thick film gold metallizations and stored for extended times at moderate temperatures. Conclusions are reached concerning the effects of conductor surface topography, thickness, and purity on bond reliability.

11729

Kossowsky, R. (Westinghouse Res. Labs., Pittsburgh, PA) and Robinson, A.I. (Westinghouse Elec. Corp., Lima, OH)
INVESTIGATION INTO FAILURES OF AL WIRES BONDED TO AU METALLIZATION IN MICROSUBSTRATES. 14th Annual Proceedings, Reliability Physics 1976

The microstructural characteristics of Al-wire bonds to Au metallization were investigated using SEM and Auger spectroscopy. Poor initial bond strength and failure of the bond after H_2 brazing cycle is attributed to impurities in the Au inks, These impurities form brittle intermetallics with Al and brittle, readily reducible, low melting glasses. The water vapor pressure created after the H_2 cycle is high enough to lift the initially ppor bond.

11730

Martin, B.D. (IBM, Hopewell Junction, NY)
DESIGN AND USE OF A LASER INTERFEROMETER FOR ULTRASONIC BONDING STUDIES. 14th Annual Proceedings, Reliability Physics 1976

An inexpensive in-line laser interferometer has been designed and built for studying ultrasonic bonding phenomena. Construction details are presented. Two applications are discussed: measurement of relative motion at the wire-bonding pad interface, and transverse motion of a wire during ultrasonic bonding.

11731

Harman, G.G. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Washington, D.C.)
THE USE OF ACOUSTIC EMISSION AS A NON-DESTRUCTIVE TEST FOR BEAM LEAD BOND INTEGRITY. 14th Annual Proceedings, Reliability Physics 1976

The use of acoustic emission (AE) as a non-destructive test to determine beam lead integrity has been investigated. Devices with one or more poorly bonded beams were mechanically stressed by pushing or pulling the die with a probe that is also an acoustical waveguide and detector. Various AE waveform signatures were obtained for specific poorly bonded beams.

11732

Spriggs, R.S. and Cronshagen, A.H. (Aerojet Electro-Systems Co., Azusa, CA)
NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC CHIP CAPACITORS FOR DELAMINATIONS AND VOIDS. 14th Annual Proceedings, Reliability Physics 1976

This paper discusses x-ray radiographic examination as a technique for detecting internal construction defects in ceramic capacitors. The methodology used, equipment requirements, critical beam and capacitor orientation parameters, minimum detectable void and plate separation and a comparison with cross sectioning technique is presented. Also discussed is the accept/reject criteria used for x-ray examination of voids and the results of accelerated life tests conducted on capacitors by x-ray grading to have varying degrees of voids.

11733

Kenney, G.B. (MIT, Cambridge, MA) and Jones, W.K. (C.S. Draper Lab., Inc., Cambridge, MA)
FUSING MECHANISM OF NICHROME RESISTOR LINKS IN PROGRAMMABLE READ-ONLY MEMORIES (PROM) DEVICES. 14th Annual Proceedings, Reliability Physics 1976

PROMs from four commercial vendors have been analyzed by transmission electron microscopy. High resolution photomicrographs and chemical analysis of the reaction products generated during the fusing operation have been obtained. A fusing model, based on the prinicples of liquid sheet disintegration, has been developed to predict the structure found within the gap region.

11734

Davidson, J.L., Gibson, J.D., Harris, S.A. and Rossiter, T.J. (Harris Semiconductor, Melbourne, FL)
FUSING MECHANISMS OF NICHROME THIN FILMS. 14th Annual Proceedings, Reliability Physics 1976

This paper will discuss the physical and chemical properties of nichrome as a thin film fusible material. Several physical models of fusing will be discussed from a theoretical standpoint. One of the models is shown consistent with experimental data which includes TEM analysis of fuse gap microstructures. Based on a physical understanding of the fusing mechanism, programming conditions that achieve the most reliable fuse gap structure will be presented.

11735

Marques, A.M. and Partridge, J. (C.S. Draper Lab., Inc., Cambridge, MA)
PROGRESS REPORT ON NiCr PROM RELIABILITY STUDIES. 14th Annual Proceedings, Reliability Physics 1976

An in progress report on the relation of programming conditions, yield, electrical test and burn-in screening, to PROM reliability history and regrow failures is presented. Data relating to the prevalent theories of the regrow mechanism is given along with programming and processing procedures found, to date, to contribute to regrow failures.

11736

Kahng, D. (Bell Labs,, Murray Hill, NJ)
DUAL DIELECTRIC CHARGE STORAGE NON-VOLATILE MEMORY CELLS. 14th Annual Proceedings, Reliability Physics 1976

It is shown that when suitable interfacial dopants such as w are introduced in a well-defined concentration range, the right-erase characteristic of dual-dielectric charge-storage cells are enormously improved. The upper limit of the dopant is dictated by its influence on the dielectirc properties of the outer layer and is determined to lie at about 10^{15} per centimeter square for Al_2O_3. Cells with $5x10^{15}$ per square centimeter interfacial dopants showed marked increase in charge leakage. The lower limit is determined to lie at about 10^{14} per square centimeter by comparison with cells with no interfacial dopants. The improvement in right-erase characteristics of these cells is of such a magnitude as to allow using relatively thick silicon-dioxide layers (greater than 50 Å). This study indicates that cells with thinner outer layers that would operate at gate-pulse voltages in the 25V, 1 microsecond range, should be feasible.

11737

Rosenberg, S. (Intel Corp., Santa Clara, CA)
POLYSILICON FUSE RELIABILITY. 14th Annual Proceedings, Reliability Physics 1976

This paper defines the major failure mechanisms associated with polysilicon fuse PROMs. High temperature accelerated lifetests are used to observe the predominant cause of device failures. Two 85°C systems were built to determine the occurrence of these failures during normal device operation.

11738

Gear, G. (Intel Corp., Santa Clara, CA)
FAMOS PROM RELIABILITY STUDIES. 14th Annual Proceedings, Reliability Physics 1976

Since the introduction of the UV erasable MOS PROM utilizing the floating gate "FAMOS" transistor cell, little device reliability data has been available. This paper presents data oriented reliability studies on the P-Channel FAMOS PROM. High temperature bakes were used to determine charge loss mechanisms and characteristic activation energy. High temperature operating lifetests and systems use data were utilized to determine retention times and component failure rates.

11739

Brockhoff, W.R. (Intersil, Inc., Cupertino, CA)
ELECTRICALLY SHORTED SEMICONDUCTOR JUNCTIONS UTILIZED AS PROGRAMMABLE READ-ONLY MEMORY ELEMENTS. 14th Annual Proceedings, Reliability Physics 1976

Occasionally a problem becomes a solution. In search of a reliable element to use as the electrically alterable storage element in a programmable read-only memory (P-ROM) the well-known failure mode of the shorted semiconductor junction was studied. Since a shorted junction is "easily produced" and remains shorted indefinitely, it can be used as a reliable P-ROM storage element. This paper describes the programming technique and summarizes over two years of reliability characterizations performed on actual P-ROM devices produced using this technique.

11740

Franklin, P. (Monolithic Memories, Inc., Sunnyvale, CA)
A RELIABILITY ASSESSMENT OF BIPOLAR PROM's 14th Annual Proceedings, Reliability Physics 1976

Design factors effecting the reliability of Schottky T^2L PROM's are discussed with special attention to the high voltage programming circuitry and fuse design. Key process controls during nichrome deposition, fuse delineation (masking) and subsequent processing environments have been developed as a result of device failure analysis. Approaches to functional and AC testing before actual programming are detailed with respect to the use of additional test "bit" and "word" lines and device design layout. One pulse programming of extra test fuses in each device is used as a special manufacturing screen to remove would be failures. "User" liabilities involved in programming, testing and Hi-Rel processing are explored with emphasis on long term reliability.

11741

Vanderkooi, N. and Riddell, M.N. (Allied Chem. Corp., Morristown, NJ)
DYNAMIC PERMEABILITY METHOD FOR EPOXY ENCAPSULATION COMPOUNDS. 14th Annual Proceedings, Reliability Physics 1976

Water vapor permeability through semiconductor encapsulation, a fundamental mechanism leading to device failure, requires an adequate permeation test to evaluate and develop improved reliability encapsulation materials. The test must overcome the limitations of current standard tests and be capable of measuring permeability and diffusion coefficients rapidly over a range of temperature, permeants and thicknesses typical of device operating conditions. This paper demonstrates the application of such a test to the development of epoxy encapsulation compounds.

11742

Wakashima, Y., Inayoshi, H., Nishi, K. and Nishida, S. (Hitachi, Ltd., Tokyo, Japan)
A STUDY OF PARASITIC MOS FORMATION MECHANISM IN PLASTIC-ENCAPSULATED MOS DEVICES. 14th Annual Proceedings, Reliability Physics 1976

With a view to eliminating parasitic MOS formation in plastic encapsulations, we studied its mechanism and found in depends not only on surface charge but also on bulk charge in plastic materials. Electrical measurements and XMA analysis revealed the charge carrier to consist of certain negative ions containing chlorine.

11743

Gregor[illegible]sch, A.J. [illegible]M, Essex Junction, VT)
POLY[illegible]DE PASSIVATION RELIABILITY STUDY. 14th [illegible]nual Proceedings, Reliability Physi[illegible] 1976

[illegible]pletely cured polyimide, in direct [illegible] with the surface of an n-channel [illegible] memory array chip, is shown to exhibit a propensity toward quasi surface inver[illegible] From the Arrhonius model, an activation energy of 1.1 eV for this phenomena is calculated. A molecular linkage related dipole theory explaining this behavior is presented and correlated with dissipation factor versus cure temperature/time curves obtained via mercury probe and aluminum dot techniques. Correlation is also made to 10K power-on-hour 85°C reliability stress data showing the inverse dependency of time-to-fail on dissipation factor.

11744

Woodard, J. (Dexter Corp., Olean, NY)
THERMALLY STIMULATED DISCHARGE EFFECTS IN POLYMER ENCAPSULANTS. 14th Annual Proceedings, Reliability Physics 1976

Regions of polymer encapsulant formulations are frequently and simultaneously exposed to high temperatures and high electric field strengths when used in encapsulation of semiconductor devices. The relatively new technique of thermally stimulated discharge is used to study the effects of these polarizing fields on various epoxy compounds. The dependence of the unique discharge curve shapes found for these systems on chemical composition is noted. Evidence is presented to indicate new and correct methods of analysis. Finally, desirable polarization properties for an epoxy encapsulant are defined, and an approach to the development of systems exhibiting these desirable properties is outlined.

11745

Fitch, W.T. (Motorola, Inc., Phoenix, AZ)
EXTENDED TEMPERATURE CYCLING OF PLASTIC AND CERAMIC IC'S WITH THERMAL SHOCK PRECONDITIONING. 14th Annual Proceedings, Reliability Physics 1976

This paper reports the results of an RADC-supported investigation to determine if an interaction between 15 cycles of thermal shock preconditioning and 3,000 cycles of temperature cycling could be observed. Four plastic DIP, three hermetic flat packages and four ceramic DIP were compared. The results of the matrix experiment were anlayzed by Analysis of Variance. Comparisons from the analysis are given and failure mode and mechanisms discussed.

KEYWORD IN CONTEXT INDEX

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11234	1969 PROCEEDINGS OF TECHNICAL PROGRAM - NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE
11359	1973 SYMPOSIUM ON SEMICONDUCTOR MEMORY TESTING - DIGEST OF TECHNICAL PAPERS
11568	1974 INTERNATIONAL MICROELECTRONIC SYMPOSIUM
11689	1975 ANNUAL RELIABILITY AND MAINTAINABILITY SYMPOSIUM ,PROCEEDINGS
11508	1975 IC APPLICATIONS CONFERENCE
11518	1975 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS
11687	1975 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,PROCEEDINGS OF TECHNICAL PROGRAM -
11535	1975 INTERNATIONAL ELECTRON DEVICES MEETING
11433	1975-13TH ANNUAL RELIABILITY PHYSICS PROCEEDINGS
11718	1976-14TH ANNUAL PROCEESINGS RELIABILITY PHYSICS
11469	ABSORPTION IN CVD BOROSILICATE GLASS-FILMS ,WATER
11476	ACCELERATED LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING METHODS ,EVALUATION OF HIGH-TEMPERATURE
11465	ACCELERATED STRESSING ,DETERMINATION OF USEFUL LIFE OF 2-LAYER METALLIZATION SYSTEMS VIA
11089	ACCELERATED TESTING OF IC'S ,PRESENT-DAY STATUS OF
11301	ACCELERATED TESTS ,METHODS FOR PLANNING AND ANALYZING
11698	ACCELERATED-AGING,STRENGTH OF GOLD-PLATED COPPER LEADS ON THIN-FILM CIRCUITS UNDER
11461	ACCELERATED TESTING,PRACTICAL APPLICATIONS OF
11463	ACCELERATED TESTING,PRACTICAL USES OF
11462	ACCELERATED TESTING,PROCESS CONTROL BY MEANS OF
11267	ACCESS 1024-BIT MEMORY MADE WITH ELECTRON LITHOGRAPHY ,HIGH-SPEED P-CHANNEL RANDOM
11058	ACCESS ,1024-BIT ECL PROM WITH 15-NS
11616	ACCURACY PRECISION AND REPEATABILITY WITH RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS ,MEASUREMENT
11148	ACCURATE METALLIZATION CAPACITANCES FOR IC'S AND PACKAGES
11603	ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO
11692	ACHIEVE RELIABILITY AND LONG LIFE ,MICROCIRCUIT PACEMAKER SPACE AGE SPIN-OFF TO
11731	ACOUSTIC EMISSION AS NON-DESTRUCTIVE TEST FOR BEAM-LEAD BOND INTEGRITY ,USE OF
11695	ACQUISITION AND TECHNOLOGY ,MILITARY IC STANDARDIZATION
11722	ACTION IN IGFET DEVICE ,RELIABILITY IMPLICATIONS OF HOT ELECTRON GENERATION AND PARASITIC BIPOLAR
11543	ACTIVE CIRCUIT AREA ,USE OF POWER TRANSFORMATION TO MODEL YIELD OF IC'S AS FUNCTION OF
11613	ACTIVE LASER-TRIMMER FOR PRODUCTION TRIMMING OF FUNCTIONAL HYBRID MICROCIRCUITS
11540	ACTIVE SEMICONDUCTOR DEVICES ,LASER SCANNING OF
11469	ADDRESSABLE CCD MEMORY ,8192-BIT BLOCK
11432	ADDRESSABLE PAM ,CCD LINE
11714	ADHESION MECHANISMS IN THICK-FILMS AND THIN-FILMS ,BASIC
11328	ADHESIVES AND ORGANIC COATINGS IN HYBRIDS ,DESIGN GUIDELINES FOR USE OF
11507	ADVANCED CMOS CIRCUIT TECHNIQUES
11317	ADVANCED CMOS CIRCUIT TECHNOLOGY
11390	ADVANCES AND APPLICATIONS ,RECENT SOS TECHNOLOGY
11537	ADVANCES IN HIGH-FREQUENCY FET'S ,RECENT
11190	ADVANCES IN MONOLITHIC OP-AMP DESIGN ,RECENT
11109	ADVANCES IN SOLDER GLASS TECHNOLOGY
11685	AEROSPACE COMPUTERS - PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS ,MOS LSI FOR
11194	AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR PRESENTATION ,GENERAL ELECTRIC
11477	AFFECTING AVALANCHE INJECTION INTO INSULATING LAYERS FROM SEMICONDUCTOR SURFACE ,FACTORS
11591	AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE
11692	AGE SPIN-OFF TO ACHIEVE RELIABILITY AND LONG LIFE ,MICROCIRCUIT PACEMAKER SPACE
11511	AGE ,BIPOLAR MEMORY COMES OF
11665	AGE ,CMOS STANDARD-PARTS LINE COMES OF
11491	AIR ISOLATION ,ISOLATION TECHNIQUES FOR FABRICATING IC'S - DIELECTRIC REFILL TECHNIQUES AND DECAL
11391	ALIGNMENT ,AUTOMATIC OUT-OF-CONTACT MASK
11700	ALTERNATE MATERIALS ,GOLD CONNECTOR CONTACTS - DEVELOPMENT IN SEARCH FOR
11070	ALTERNATIVE TO SEMICONDUCTORS FOR FAST COMPUTER CIRCUITS ,SUPERCONDUCTING TUNNEL DEVICES AS
11134	ALUMINA SILICON-DIOXIDE GATE DIELECTRICS ,RADIATION RESISTANCE OF CMOS CIRCUITS MADE WITH
11254	ALUMINA SILICON-DIOXIDE SILICON FET ,STUDY OF CHARGE STORAGE BEHAVIOR IN METAL
11402	ALUMINA SILICON-DIOXIDE SILICON ,POLARIZATION AND CHARGE MOTION IN METAL
11243	ALUMINA SUBSTRATES RELIABILITY CRITERIA- USER VIEW-POINT
11449	ALUMINUM AND GOLD METAL SYSTEMS ,EFFECTS OF FAST TEMPERATURE CYCLING ON
11139	ALUMINUM CANTILEVERED BEAMS ,FLEXIBLE MULTILAYER INTERCONNECTION USING EVAPORATED
11349	ALUMINUM ELECTROMIGRATION FAILURE STUDIES ,PRACTICAL PROBLEMS IN APPLICATION OF
11141	ALUMINUM INTERCONNECTS FOR MSI AND LSI ,ENGINEERING STUDY OF DEVELOPMENT O- 2-LEVEL ANODIZED
11727	ALUMINUM INTERMETALLICS ON THIN-FILM HYBRID MICROCIRCUIT SUBSTRATES ,GOLD
11725	ALUMINUM METALLIZATION ,EFFECT OF IMPURITIES ON CORROSION OF
11640	ALUMINUM THIN-FILMS ON SEMICONDUCTOR DEVICES ,REVIEW OF LIMITATIONS OF

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11103	ALUMINUM THIN-FILMS UNDER CONSTANT AND REVERSED DC POWERING ,ELECTROMIGRATION FAILURE IN
11591	ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF
11728	ALUMINUM WIRE BONDS TO GOLD METALLIZATION ,METALLURGICAL ASPECTS OF
11729	ALUMINUM WIRES BONDED TO GOLD METALLIZATION IN MICROSUBSTRATES ,INVESTIGATION INTO FAILURES OF
11453	ALUMINUM-COPPER AL-CU-SI AND SILVER CONDUCTORS ,WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN
11046	AMPLIFIER IN CCD'S ,DISTRIBUTED FLOATING-GATE
11135	AMPLIFIER WITH OCTAVE BANDWIDTH ,UHF HYBRID INTEGRATED 45-WATT 2-STAGE
11473	AMPLIFIER ,DESIGN AND OPERATION OF FLOATING GATE
11407	AMPLIFIER ,DEVELOPMENT OF HIGH RELIABILITY RF KEYED CROSSED FIELD
11133	AMPLIFIER ,RADIATION TOLERANT GATED VIDEO
11136	AMPLIFIER-LIMITER,INTEGRATED INTERMEDIATE FREQUENCY
11674	ANALOG APPLICATIONS ,CMOS PLL - VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND
11069	ANALOG CCD FOR TIME SHARED RECURSIVE FILTERS ,DUAL DIFFERENTIAL
11051	ANALOG MULTIPLEXER ,JFET BIPOLAR 8-CHANNEL
11065	ANALOG PROCESSOR ,SERIAL
11490	ANALOG SIGNAL PROCESSING ,CCD
11318	ANALOG SIGNAL PROCESSING ,CCD'S MOVE-IN ON MEMORIES AND
11703	ANALOG SIGNAL PROCESSING ,CCD'S IN
11067	ANALOG SIGNAL PROCESSING ,REPROGRAMMABLE FILTER BANK USING CCD DISCRETE
11513	ANALOG SWITCH ,APPLICATIONS OF 10-OHM HIGH-SPEED
11412	ANALOG SWITCHES AND MULTIPLEXERS ,FOCUS ON IC
11675	ANALYSER USING HELIUM-NEON LASER ,SILICON SLICE
11361	ANALYZING ACCELERATED TESTS ,METHODS FOR PLANNING AND
11425	ANGLE MEASUREMENTS ,CHARACTERIZATION OF THERMALLY GROWN SILICON-DIOXIDE SURFACES BY CONTACT
11641	ANNEALING TREATMENTS ON CHARGE TRAPPING IN CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION
11284	ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT SINKS ,THERMAL PROPERTIES OF
11141	ANODIZED ALUMINUM INTERCONNECTS FOR MSI AND LSI ,ENGINEERING STUDY OF DEVELOPMENT OF 2-LEVEL
11603	ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS
11653	APPEARANCE POTENTIAL SPECTROSCOPY ,INVESTIGATION OF SURFACE OXIDE LAYERS BY X-RAY
11500	APPROACHES FOR IMPROVING PRODUCT RELIABILITY THROUGH RELIABILITY PHYSICS TECHNIQUES ,STUDY OF
11701	APPROACHES TO HIGH-VOLUME IC PRODUCTION ,FILM CARRIER
11068	ARCHITECTURE ,RAZORBACK CCD - HIGH-PERFORMANCE PARALLEL INPUT DELAY LINE
11219	ARE FACTS ,BEAM-LEADS - WHAT
11170	AREA BY ONE-THIRD ,FIRST OXIDE ISOLATED CMOS CIRCUITS CUT CHIP
11543	AREA ,USE OF POWER TRANSFORMATION TO MODEL YIELD OF IC'S AS FUNCTION OF ACTIVE CIRCUIT
11284	ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT SINKS ,THERMAL PROPERTIES OF ANNULAR AND
11137	ARRAY RADAR APPLICATIONS ,HYBRID INTEGRATED FERRITE PHASE-SHIFTER DRIVER FOR PHASED
11510	ARRAY ,FIELD PROGRAMMABLE LOGIC
11049	ARRAY ,TRANSPARENT METAL OXIDE ELECTRODE CID IMAGER
11610	ARRAYS FOR EFFICIENT HYBRID PACKAGING ,COMPLEX BEAM-LEADED LOGIC AND MEMORY
11157	ARRAYS FOR SPACE STATION ,DESIGN PROCESSING AND TESTING OF LSI
11652	ARRAYS IN ESFI MOS TECHNOLOGY ,FULLY DECODED MNOS STORAGE
11367	ARRAYS ,EFFICIENT TESTING OF COMBINATIONAL LOGIC CELLS IN LARGE-SCALE
11258	ARRAYS ,INTERGRATED MONOLITHIC PHOTOSENSOR
11052	A/D-CONVERTER ,HIGH-PRECISION [illegible]ENT TOLERANT
11516	A/D-CONVERTERS ,APPLICATIONS OF [illegible]AMP
11608	ASSEMBLIES ,SPOT IN-LINE QUALITY CO[illegible]L SYSTEM FOR HYBRID MICROELECTRONIC
11633	ASSEMBLIES ,TESTERS - COMPONENTS IC'S PC-CARDS
11582	ASSEMBLY AND TEST OF HYBRIDS ON EPOXY-FIBER GLASS SUBSTRATES ,FABRICATION
11371	ASSEMBLY OF HYBRID IC'S ,PRODUCTION ENGINEERING MEASURES AUTOMATIC
11260	ASSEMBLY TECHNIQUES ,MICROCIRCUIT PACKAGES AND
11235	ASSEMBLY ,INFARED HEATING APPLICATIONS IN MICROCIRCUIT
11740	ASSESSMENT OF BIPOLAR PROM'S ,RELIABILITY
11632	ASSESSMENT - SCREENPRINTING THICK-FILM ,TECHNOLOGY
11281	ATMOS - ELECTRICALLY REPROGRAMMABLE ROM DEVICE
11600	ATMOSPHERE IN HERMETICALLY SEALED SEMICONDUCTOR PACKAGES ,MEASUREMENT AND CONTROL OF
11457	ATTACH FOR HYBRID FABRICATION ,MULTILEVEL SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT
11578	ATTACHMENT WITH SMALL BUMP FLIP-CHIPS ,SEMICONDUCTOR CHIP
11622	ATTENUATED TOTAL INFRARED INTERNAL REFLECTION FOR CHARACTERIZATION OF ELECTRONIC FILMS
11650	AUTOMATED CONTROLS FOR CONTINUOUS EPITAXIAL PROCESSING OF SILICON IC'S ,MANUFACTURING METHODS TECHNIQUES AND
11392	AUTOMATED METAL ETCH SYSTEM FOR IC MANUFACTURE
11371	AUTOMATIC ASSEMBLY OF HYBRID IC'S ,PRODUCTION ENGINEERING MEASURES
11480	AUTOMATIC DIELECTRIC QUALITY EVALUATING SYSTEM
11391	AUTOMATIC OUT-OF-CONTACT MASK ALIGNMENT
11627	AUTOMATIC TESTING OF INCOMING DIGITAL DEVICES

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11376	BRITISH NATIONAL SPACEPROGRAM ,HYBRID MICROCIRCUIT TECHNOLOGY IN
11430	BUBBLE MEMORY CHIPS ,FABRICATION OF
11145	BUBBLE MEMORY STATUS AND TRENDS IN US-GOVERNMENT DATA STORAGE APPLICATIONS
11245	BUBBLE MEMORY ,MAGNETIC
11090	BUBBLES DURING DEVITRIFICATION AND REMELTING OF CRYSTALS IN GLASS ,FORMATION OF
11674	BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS ,CMOS PLL - VERSATILE
11322	BULK-TRANSFER CCD'S ,MEASUREMENTS ON DEPLETION-MODE FET'S AND
11577	BUMP FLIP-CHIP FABRICATION USING CIRCUIT LAYOUT ,SOLDER
11578	BUMP FLIP-CHIPS ,SEMICONDUCTOR CHIP ATTACHMENT WITH SMALL
11239	BUMPS FOR FACE-DOWN BONDING OF HYBRID COMPONENTS ,PREPARATION OF SUBSTRATES WITH
11569	BURIED-LAYER THIN-FILM PASSIVATION ,TITANIUM NITROXIDE
11295	BURNOUT OF IC'S ,PULSED-POWER
11591	BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER
11679	BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON
11452	BUTTINGCONTACTS ,FAILURE MECHANISM OF METAL-POLYSILICON DOPED SILICON
11586	CALIBRATION OF THICK-FILM RESISTOR PASTES BY WEIGHT
11130	CAMERAS THROUGH HYBRID IC TECHNOLOGY , MINIATURIZATION OF TELEVISION
11139	CANTILEVERED BEAMS ,FLEXIBLE MULTILAYER INTERCONNECTION USING EVAPORATED ALUMINUM
11411	CAPABILITY FOR BEAM-LEAD DEVICES ,DEVELOPMENT OF COMPLIANT BONDING
11148	CAPACITANCES FOR IC'S AND PACKAGES ,ACCURATE METALLIZATION
11575	CAPACITOR CHIPS FOR HYBRID CIRCUITS - MANUFACTURING PROCESS ,MULTILAYER CERAMIC
11732	CAPACITORS FOR DELAMINATIONS AND VOIDS ,NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC CHIP
11291	CAPACITORS ,EFFECTS OF DISLOCATIONS ON PROPERTIES OF METAL SILICON-DIOXIDE
11271	CAPACITORS ,NON-EQUILIBRIUM PHENOMENA IN ION-IMPLANTED MOS
11701	CARRIER APPROACHES TO HIGH-VOLUME IC PRODUCTION ,FILM
11593	CASE FOR BETTER EPOXY PERFORMANCE TESTING AND NEED FOR STANDARDIZED FORMULATIONS
11158	CAUSES AND CURES ,COMPONENT INFANT-MORTALITY -
11072	CCCL ,NEW APPROACH TO BIPOLAR LSI -
11490	CCD ANALOG SIGNAL PROCESSING
11499	CCD CONCEPT ,EXPERIMENTAL VERIFICATION OF
11066	CCD DELAY LINE ,MULTIPLEXED VIDEO BANDWIDTH
11067	CCD DISCRETE ANALOG SIGNAL PROCESSING ,REPROGRAMMABLE FILTER BANK USING
11069	CCD FOR TIME SHARED RECURSIVE FILTERS ,DUAL DIFFERENTIAL ANALOG
11539	CCD IMAGERS
11432	CCD LINE ADDRESSABLE RAM
11683	CCD MEMORY SYSTEM ,DESIGN AND PERFORMANCE OF
11365	CCD MEMORY WITH MNOS STORAGE ,NON-VOLATILE
11469	CCD MEMORY ,8192-BIT BLOCK ADDRESSABLE
11068	CCD - HIGH-PERFORMANCE PARALLEL INPUT DELAY LINE ARCHITECTURE ,RAZORBACK
11395	CCD SIGNAL PROCESSORS
11492	CCD TRANSFER USING IMPULSE AND FREQUENCY RESPONSES ,MEASUREMENT OF CHARGE RESIDUAL FOR
11495	CCD'S
11703	CCD'S IN ANALOG SIGNAL PROCESSING
11318	CCD'S MOVE-IN ON MEMORIES AND ANALOG SIGNAL PROCESSING
11679	CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL
11046	CCD'S ,DISTRIBUTED FLOATING-GATE AMPLIFIER IN
11368	CCD'S ,INFLUENCE OF CLOCK WAVEFORMS ON PERFORMANCE OF
11263	CCD'S ,LINEARITY OF ELECTRICAL CHARGE-INJECTION INTO
11372	CCD'S ,MEASUREMENTS OF NOISE IN
11322	CCD'S ,MEASUREMENTS ON DEPLETION-MODE FET'S AND BULK-TRANSFER
11268	CCD'S ,STRUCTURE DEPENDENCE OF FREE CHARGE-TRANSFER IN
11232	CCD'S ,SURFACE POTENTIAL EQUILIBRATION METHOD OF SETTING CHARGE IN
11303	CELLS FOR FAST DENSE MEMORIES ,ISOLATION METHOD SHRINKS BIPOLAR
11367	CELLS IN LARGE-SCALE ARRAYS ,EFFICIENT TESTING OF COMBINATIONAL LOGIC
11736	CELLS ,DUAL DIELECTRIC CHARGE STORAGE NON-VOLATILE MEMORY
11575	CERAMIC CAPACITOR CHIPS FOR HYBRID CIRCUITS - MANUFACTURING PROCESS ,MULTILAYER
11732	CERAMIC CHIP CAPACITORS FOR DELAMINATIONS AND VOIDS ,NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF
11745	CERAMIC IC'S WITH THERMAL-SHOCK PRECONDITIONING ,EXTENDED TEMPERATURE CYCLING OF PLASTIC AND
11619	CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON
11655	CERAMICS ,COMPOSITE FILM METALLIZING FOR
11591	CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD
11661	CHARACTERISTICS AND MECHANISMS OF OPTICALLY-COUPLED ISOLATOR ,DEGRADATION
11429	CHARACTERISTICS FOR MIL-STD-883 ,NEW RECOMMENDATION METHOD-1012 - THERMAL
11272	CHARACTERISTICS OF BORON-IMPLANTED N-CHANNEL MOS TRANSISTORS ,ELECTRICAL
11131	CHARACTERISTICS OF HARDENED DIGITAL IC FAMILY ,RADIATION
11651	CHARACTERISTICS ,DEPENDENCE OF SILICON-NITRIDE FILM THICKNESS ON BIPOLAR TRANSISTOR
11567	CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES
11680	CHARACTERIZATION OF DEFECTS IN SILICON P-N JUNCTIONS ,THERMALLY STIMULATED MEASUREMENTS

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11622 CHARACTERIZATION OF ELECTRONIC FILMS ,ATTENUATED TOTAL INFRARED INTERNAL REFLECTION FOR
11408 CHARACTERIZATION OF LOCALIZED DEFECTS IN DIELECTRIC FILMS ,DETECTION AND
11538 CHARACTERIZATION OF PLASMA ETCHING FOR SEMICONDUCTOR APPLICATIONS
11609 CHARACTERIZATION OF POLYMERIC MATERIALS USED IN MICROELECTRONIC DEVICE BONDING
11425 CHARACTERIZATION OF THERMALLY GROWN SILICON-DIOXIDE SURFACES BY CONTACT ANGLE MEASUREMENTS
11605 CHARACTERIZATION OF THERMOCOMPRESSION BONDING PARAMETERS FOR BEAM-LEAD BONDING
11570 CHARACTERIZATION OF THICK-FILM FRITLESS METALIZATION
11232 CHARGE IN CCD'S ,SURFACE POTENTIAL EQUILIBRATION METHOD OF SETTING
11721 CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF SURFACE
11402 CHARGE MOTION IN METAL ALUMINA SILICON-DIOXIDE SILICON ,POLARIZATION AND
11492 CHARGE RESIDUAL FOR CCD TRANSFER USING IMPULSE AND FREQUENCY RESPONSES ,MEASUREMENT OF
11254 CHARGE STORAGE BEHAVIOR IN METAL ALUMINA SILICON-DIOXIDE SILICON FET ,STUDY OF
11736 CHARGE STORAGE NON-VOLATILE MEMORY CELLS ,DUAL DIELECTRIC
11195 CHARGE TRANSPORT AND POLARIZATION EFFECTS IN DIELECTRICS OF MSI AND LSI DEVICES
11641 CHARGE TRAPPING IN CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON
11555 CHARGED-COUPLED FET DEVICES
11263 CHARGE-INJECTION INTO CCD'S ,LINEARITY OF ELECTRICAL
11266 CHARGE-TRANSFER DEVICES ,THEORY OF NOISE IN
11268 CHARGE-TRANSFER IN CCD'S ,STRUCTURE DEPENDENCE OF FREE
11061 CHARGE-TRANSFER SENSE-AMPLIFIER ,HIGH-SENSITIVITY
11447 CHEMICAL ASPECTS OF FAILURE MECHANISM ,MIGRATORY GOLD RESISTANCE SHORTS -
11712 CHEMICAL CLEANING FOR THERMOCOMPRESSION BONDING ,ON
11170 CHIP AREA BY ONE-THIRD ,FIRST OXIDE ISOLATED CMOS CIRCUITS CUT
11578 CHIP ATTACHMENT WITH SMALL BUMP FLIP-CHIPS ,SEMICONDUCTOR
11732 CHIP CAPACITORS FOR DELAMINATIONS AND VOIDS ,NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC
11238 CHIP JOINING ,MODULE MATERIALS FOR CONTROLLED COLLAPSE
11329 CHIP MOUNTING TECHNOLOGY FOR HYBRIDS ,INVESTIGATION OF DISCRETE COMPONENT
11576 CHIP RESISTORS ,ULTRA LOW-OHM
11631 CHIP ,LASER-TRIMMING ON
11085 CHIP ,MINICOMPUTER ON
11575 CHIPS FOR HYBRID CIRCUITS - MANUFACTURING PROCESS ,MULTILAYER CERAMIC CAPACITOR
11357 CHIPS WITH CONDUCTIVE EPOXIES ,BOND
11430 CHIPS ,FABRICATION OF BUBBLE MEMORY
11724 CHIPS ,MICROSURGERY AS TOOL IN ANALYSIS OF LSI SILICON
11049 CID IMAGER ARRAY ,TRANSPARENT METAL OXIDE ELECTRODE
11048 CID ,3-TERMINAL
11375 CIRCUIRTY-VOL-I ,HARDENED MOS INPUT AND OUTPUT
11543 CIRCUIT AREA ,USE OF POWER TRANSFORMATION TO MODEL YIELD OF IC'S AS FUNCTION OF ACTIVE
11138 CIRCUIT DESIGN ,DIAMOND - NEW APPROACH TO MICROELECTRONIC
11251 CIRCUIT DESIGN ,SOS MOS MODELING FOR
11075 CIRCUIT FOR TV RECEIVERS USING IIL TECHNIQUES ,VERTICAL SYNCHRONIZING
11577 CIRCUIT LAYOUT ,SOLDER BUMP FLIP-CHIP FABRICATION USING
11601 CIRCUIT MANUFACTURER ,FRUSTRATIONS OF LOW COST PACKAGING AS SEEN BY HYBRID
11127 CIRCUIT MATERIALS ,EFFECTS OF HIGH ENERGY PULSES ON HYBRID
11612 CIRCUIT PACKAGING ,INTEGRAL LED DISPLAY AND DRIVE
11507 CIRCUIT TECHNIQUES ,ADVANCED CMOS
11317 CIRCUIT TECHNOLOGY ,ADVANCED CMOS
11678 CIRCUIT ,NUCLEAR RADIATION EFFECTS ON RCA ECOM LSI RADIAC COUNTER
11394 CIRCUITRY ,RADIATION RESISTANT CMOS SOS
11518 CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS ,1975 IEEE INTERNATIONAL SOLID-STATE
11170 CIRCUITS CUT CHIP AREA BY ONE-THIRD ,FIRST OXIDE ISOLATED CMOS
11720 CIRCUITS FOR BELL SYSTEM ,RELIABILITY OF IIL
11667 CIRCUITS FOR CONSUMER APPLICATIONS ,CMOS
11056 CIRCUITS FOR MARGINALLY TESTABLE 4K-RAM ,SIMPLIFIED PERIPHERAL
11179 IC'S IN PLASTIC PACKAGES ,RELIABILITY EVALUATION OF HERMETIC
11134 CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE GATE DIELECTRICS ,RADIATION RESISTANCE OF CMOS
11575 CIRCUITS - MANUFACTURING PROCESS ,MULTILAYER CERAMIC CAPACITOR CHIPS FOR HYBRID
11459 CIRCUITS - THEIR EFFECT ON RELIABILITY ,REPAIRS TO COMPLEX HYBRID
11698 CIRCUITS UNDER ACCELERATED-AGING,STRENGTH OF GOLD-PLATED COPPER LEADS ON THIN-FILM
11074 CIRCUITS ,CURRENT HOGGING INJECTION LOGIC - NEW FUNCTIONALLY INTEGRATED
11620 CIRCUITS ,ELECTRICAL SCREEN FOR HIGH-RELIABILITY HYBRID
11494 CIRCUITS ,EMP HARDENED CMOS
11276 CIRCUITS ,FEEDTHROUGH IN ECL
11644 CIRCUITS ,INFRARED SIGNATURES FOR ANALYSIS OF DIGITAL
11198 CIRCUITS ,INTEGRATED THERMIONIC
11497 CIRCUITS ,LOW-POWER HIGH-SPEED CMOS/SOS
11606 CIRCUITS ,MEASUREMENTS OF SOLDERABILITY OF THICK-FILM
11482 CIRCUITS ,PROGRAMMABLE MEMORY
11594 CIRCUITS ,SELECTION AND CONTROLS OF POLYMERS USED IN MANUFACTURE OF HYBRID
11070 CIRCUITS ,SUPERCONDUCTING TUNNEL DEVICES AS ALTERNATIVE TO SEMICONDUCTORS FOR FAST COMPUTER
11654 CLEANING BY ULTRAVIOLET RADIATION ,SURFACE
11712 CLEANING FOR THERMOCOMPRESSION BONDING ,ON CHEMICAL
11424 CLEANING OF METAL SURFACES ,PLASMA

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11368 CLOCK WAVEFORMS ON PERFORMANCE OF CCD'S ,INFLUENCE OF
11047 CLOCK-PULSELESS SCANNER FOR MOS IMAGE SENSORS ,ULTRA HIGH-SPEED
11275 CMOS AND COMPLEMENTARY ISOLATED BIPOLAR TRANSISTOR MONOLITHIC INTEGRATION PROCESS
11509 CMOS AND MICROPROCESSOR SYSTEMS ,USING BIPOLAR LOGIC TO IMPROVE PERFORMANCE IN
11507 CMOS CIRCUIT TECHNIQUES ,ADVANCED
11317 CMOS CIRCUIT TECHNOLOGY ,ADVANCED
11170 CMOS CIRCUITS CUT CHIP AREA BY ONE-THIRD ,FIRST OXIDE ISOLATED
11667 CMOS CIRCUITS FOR CONSUMER APPLICATIONS
11134 CMOS CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE GATE DIELECTRICS ,RADIATION RESISTANCE OF
11494 CMOS CIRCUITS ,EMP HARDENED
11669 CMOS CUSTOM DESIGN ,DOING YOUR OWN THING -
11670 CMOS IC'S IN AUTOMOBILE ENVIRONMENT
11261 CMOS IC'S ,LATCH-UP IN

11565 CMOS IC'S ,LIMITATIONS ON MAXIMUM OPERATING VOLTAGE OF
11201 CMOS IC'S ,RELIABILITY OF
11699 CMOS IC'S ,TOTAL-DOSE RADIATION HARDENED
11673 CMOS IS HIGH-RELIABILITY TECHNOLOGY
11143 CMOS MASS MEMORY ,LOW-POWER
11671 CMOS OFFER MINIMAL POWER DIGITAL DISPLAYS ,LIQUID CRYSTALS AND
11517 CMOS OP-AMP ,UNDERSTANDING AND USING UNIQUE
11557 CMOS OPTIMIZATION FOR RADIATION HARDNESS
11674 CMOS PLL - VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS
11691 CMOS - MATURING TECHNOLOGY ,COMPARATIVE RELIABILITY EVALUATION OF
11663 CMOS - RCA'S THRUST IN DIGITAL LOGIC ,MOS - RCA PIONEERED TECHNOLOGY
11666 CMOS SIMPLIFIES EQUIPMENT DESIGN
11394 CMOS SOS CIRCUITRY ,RADIATION RESISTANT
11723 CMOS SOS RELIABILITY STUDY
11710 CMOS SOS ,HIGH-SPEED
11665 CMOS STANDARD-PARTS LINE COMES OF AGE
11207 CMOS TECHNOLOGY IN COMPLEX IC'S ,RELIABILITY EVALUATION OF
11521 CMOS TECHNOLOGY ,CMOS-III - HIGH DENSITY ION-IMPLANTED
11662 CMOS TECHNOLOGY ,RCA
11668 CMOS TECHNOLOGY ,TIMEKEEPING REVOLUTION THROUGH
11255 CMOS ,SAPPHIRE BRINGS OUT BEST IN
11521 CMOS-III - HIGH DENSITY ION-IMPLANTED CMOS TECHNOLOGY
11497 CMOS/SOS CIRCUITS ,LOW-POWER HIGH-SPEED
11595 COATING FOR NON-LIDDED HYBRID MICROCIRCUITS ,CONFORMAL POLYMER
11460 COATING MATERIALS ,HYBRID TECHNOLOGY LOOSE PARTICLES AND
11478 COATING NARROW RESISTIVE LINES TO INCREASE ELECTROMIGRATION RESISTANCE
11328 COATINGS IN HYBRIDS ,DESIGN GUIDELINES FOR USE OF ADHESIVES AND ORGANIC
11642 COATINGS ON HYBRID MICROCIRCUITS ,APPROACH FOR EVALUATING POLYMER MATERIALS AS PROTECTIVE
11706 COATINGS ON SILICON DEVICES ,PASSIVATION
11238 COLLAPSE CHIP JOINING ,MODULE MATERIALS FOR CONTROLLED
11560 COLLECTOR SHORTS IN BIPOLAR DEVICES ,EMITTER
11367 COMBINATIONAL LOGIC CELLS IN LARGE-SCALE ARRAYS ,EFFICIENT TESTING OF
11567 COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH
11511 COMES OF AGE ,BIPOLAR MEMORY
11665 COMES OF AGE ,CMOS STANDARD-PARTS LINE
11304 COMING UP FAST FROM BEHIND - DENSER BIPOLAR
11562 COMMUNICATIONS ,HIGH-POWER LONG-LIVED DOUBLED HETEROSTRUCTURE LED'S FOR OPTICAL
11707 COMMUNICATIONS ,PACKET RADIO
11512 COMMUNICATIONS ,PRECISION PLL SYSTEM FOR DATA
11561 COMMUNICATIONS ,RELIABILITY SEMICONDUCTOR LIGHT SOURCES FOR FIBER OPTICAL
11691 COMPARATIVE RELIABILITY EVALUATION OF CMOS - MATURING TECHNOLOGY
11364 COMPARSION OF SEMICONDUCTING PROPERTIES OF THIN-FILMS OF SOS AND SPINEL
11523 COMPATIBLE COMPLEMENTARY PNP TRANSISTORS ,HIGH SLEW RATE MONOLITHIC OP-AMP USING
11366 COMPATIBLE MOS LOGIC ,VMOS - HIGH-SPEED TTL
11057 COMPATIBLE RAM ,4096-BIT HIGH-SPEED ECL
11564 COMPLEMENTARY DMOS PROCESS FOR LSI
11275 COMPLEMENTARY ISOLATED BIPOLAR TRANSISTOR MONOLITHIC INTEGRATION PROCESS ,CMOS AND
11523 COMPLEMENTARY PNP TRANSISTORS ,HIGH SLEW RATE MONOLITHIC OP-AMP USING COMPATIBLE
11399 COMPLETE REMOVAL OF SODIUM FROM SILICON-DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS
11610 COMPLEX BEAM-LEADED LOGIC AND MEMORY ARRAYS FOR EFFICIENT HYBRID PACKAGING
11459 COMPLEX HYBRID CIRCUITS - THEIR EFFECT ON RELIABILITY ,REPAIRS TO
11615 COMPLEX HYBRID IC'S ,HIGH-RELIABILITY
11207 COMPLEX IC'S ,RELIABILITY EVALUATION OF CMOS TECHNOLOGY IN
11693 COMPLEX MOS LSI DEVICES IN AUTOMOTIVE APPLICATION ,PREDICTING RELIABILITY OF SYSTEMS USING
11411 COMPLIANT BONDING CAPABILITY FOR BEAM-LEAD DEVICES ,DEVELOPMENT OF
11633 COMPONENTS IC'S PC-CARDS ASSEMBLIES ,TESTERS -
11239 COMPONENTS ,PREPARATION OF SUBSTRATES WITH BUMPS FOR FACE-DOWN BONDING OF HYBRID
11373 COMPONENTS ,QUALITY MEASURE FOR LSI
11597 COMPONENTS ,USE OF EPOXIES FOR HIGH-VOLUME PRODUCTION OF MICROELECTRON.
11655 COMPOSITE FILM METALLIZING FOR CERAMICS
11284 COMPOSITE HEAT SINKS ,THERMAL PROPERTIES OF ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11741	COMPOUNDS ,DYNAMIC PERMEABILITY METHOD FOR EPOXY ENCAPSULATION
11498	COMPRESSION TECHNIQUES ,FAST-SETTLING MONOLITHIC OP-AMP USING DOUBLET
11070	COMPUTER CIRCUITS ,SUPERCONDUCTING TUNNEL DEVICES AS ALTERNATIVE TO SEMICONDUCTORS FOR FAST
11362	COMPUTER DESIGN ,SURVIVABLE PMOS
11128	COMPUTER FOR SATELLITE APPLICATIONS ,GENERAL PURPOSE
11296	COMPUTER GENERATED TROUBLESHOOTING TREES - PROGRAM
11566	COMPUTER MODEL FOR LATERAL THERMAL INSTABILITIES IN POWER-TRANSISTORS
11126	COMPUTER ,UNIVERSAL PACKAGING SYSTEM AS APPLIED TO ALL APPLICATIONS DIGITAL
11672	COMPUTER-AIDED DESIGN ,KEEPING UP WITH TIMES THROUGH
11055	COMPUTER-AIDED SYNTHESIS OF IC ELECTRICAL DIAGRAM FROM MASK DATA
11409	COMPUTER-AIDED VULNERABILITY ANALYSIS OF D/A-CONVERTER
11685	COMPUTERS - PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS ,MOS LSI FOR AEROSPACE
11499	CONCEPT ,EXPERIMENTAL VERIFICATION OF CCD
11572	CONCEPT ,HIGH-TEMPERATURE VISCOSITY CONTROL IN MULTILAYER GLASSES NEW
11585	CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT
11571	CONDITIONS ,THICK-FILM MATERIAL MICROSTRUCTURE - INFLUENCE OF PROCESSING
11426	CONDUCTION AND SWITCHING IN SILICON-DIOXIDE ,ON NATURE OF
11300	CONDUCTION ELECTRONS IN N-TYPE INVERSION LAYERS IN <100>-SURFACES OF SILICON ,TRANSPORT PROPERTIES OF
11227	CONDUCTION HEAT FLOW IN SOLID-STATE DEVICES ,CTRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF
11357	CONDUCTIVE EPOXIES ,BOND CHIPS WITH
11320	CONDUCTIVITY OF EXTRINSIC SEMICONDUCTOR FILMS ,EFFECT OF SURFACE REGIONS ON ELECTRICAL
11574	CONDUCTOR RESISTOR SYSTEM USEFUL TO 6-GHZ ,PRATICAL ASPECTS IN DETERMINATION OF THICK-FILM
11448	CONDUCTORS ,ELECTROMIGRATION FAILURE IN GOLD THIN-FILM
11493	CONDUCTORS ,MULTICHIP IC MEMORY WITH PHOTOFORMED PLATED
11588	CONDUCTORS ,RELIABILITY CONSIDERATION FOR ULTRASONIC WIRE BONDING ON THICK-FILM
11453	CONDUCTORS ,WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN ALUMINUM-COPPER AL-CU-SI AND SILVER
11518	CONFERENCE DIGEST OF TECHNICAL PAPERS ,1975 IEEE INTERNATIONAL SOLID-STATE CIRCUITS
11234	CONFERENCE ,1969 PROCEEDINGS OF TECHNICAL PROGRAM - NATIONAL ELECTRONIC PACKAGING AND PRODUCTION
11508	CONFERENCE ,1975 IC APPLICATIONS
11687	CONFERENCE ,PROCEEDINGS OF TECHNICAL PROGRAM - 1975 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION
11595	CONFORMAL POLYMER COATING FOR NON-LIDDED HYBRID MICROCIRCUITS
11619	CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS
11700	CONNECTOR CONTACTS - DEVELOPMENT IN SEARCH FOR ALTERNATE MATERIALS ,GOLD
11588	CONSIDERATION FOR ULTRASONIC WIRE BONDING ON THICK-FILM CONDUCTORS ,RELIABILITY
11103	CONSTANT AND REVERSED DC POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS UNDER
11236	CONSTANT ,THICK-FILM WITH HIGH DIELECTRIC
11667	CONSUMER APPLICATIONS ,CMOS CIRCUITS FOR
11425	CONTACT ANGLE MEASUREMENTS ,CHARACTERIZATION OF THERMALLY GROWN SILICON-DIOXIDE SURFACES BY
11479	CONTACT THROUGH SILICON-DIOXIDE OVERLAY BY ULTRASONIC PROBE ,ELECTRICAL
11483	CONTACT-HOLE OPENING FOR FABRICATING SCHOTTKY-BARRIER DIODE
11700	CONTACTS - DEVELOPMENT IN SEARCH FOR ALTERNATE MATERIALS ,GOLD CONNECTOR
11287	CONTAINING BEAM-LEAD DEVICES ,DEVELOPMENT OF PROCESSES FOR HYBRID MICROCIRCUITS
11124	CONTAMINANTS ,IC PACKAGES AND HERMETICALLY SEALED-IN
11464	CONTAMINATED MICROCIRCUIT PROCESSES ,HIGH-TEMPERATURE OPERATING TESTS - CONTROL FOR
11711	CONTAMINATION ON THERMOCOMPRESSION BONDABILITY OF GOLD ,EFFECT OF SURFACE
11650	CONTINUOUS EPITAXIAL PROCESSING OF SILICON IC'S ,MANUFACTURING METHODS TECHNIQUES AND AUTOMATED CONTROLS FOR
11549	CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS ,SIMPLE ETCH
11628	CONTRACT POTENTIAL MEASUREMENTS ON THIN SILICON-DIOXIDE
11572	CONTROL IN MULTILAYER GLASSES NEW CONCEPT ,HIGH-TEMPERATURE VISCOSITY
11238	CONTROLLED COLLAPSE CHIP JOINING MODULE MATERIALS FOR
11556	CONTROLLED THYRISTOR - NEW COMPONENT ,FIELD
11650	CONTROLS FOR CONTINUOUS EPITAXIAL PROCESSING OF SILICON IC'S ,MANUFACTURING METHODS TECHNIQUES AND AUTOMATED
11594	CONTROLS OF POLYMERS USED IN MANUFACTURE OF HYBRID CIRCUITS ,SELECTION AND
11698	COPPER LEADS ON THIN-FILM CIRCUITS UNDER ACCELERATED-AGING,STRENGTH OF GOLD-PLATED
11241	CORRECTION OF MATERIALS AND PROCESSES PROBLEMS IN THIN-FILM NETWORKS ,DETECTION AND
11444	CORROSION DEGRADATION ,SUSCEPTIBILITY OF MICROWELDS IN HYBRID MICROCIRCUITS TO
11725	CORROSION OF ALUMINUM METALLIZATION ,EFFECT OF IMPURITIES ON
11419	COST AND RELIABILITY-VOL-I,STUDY OF MILITARY ELECTRONICS WITH PARTICULAR REFERENCE TO
11601	COST PACKAGING AS SEEN BY HYBRID CIRCUIT MANUFACTURER ,FRUSTRATIONS OF LOW
11678	COUNTER CIRCUIT ,NUCLEAR RADIATION EFFECTS ON RCA ECOM LSI RADIAC
11555	COUPLED FET DEVICES ,CHARGED
11378	CRACKING OF KOVAR PACKAGE LEADS ,METALLURGICAL ANALYSIS OF STRESS-CORROSION
11243	CRITERIA - USER VIEW-POINT ,ALUMINA SUBSTRATES RELIBILITY
11407	CROSSED FIELD AMPLIFIER ,DEVELOPMENT OF HIGH RELIABILITY RF KEYED
11671	CRYSTALS AND CMOS OFFER MINIMAL POWER DIGITAL DISPLAYS ,LIQUID
11090	CRYSTALS IN GLASS ,FORMATION OF BUBBLES DURING DEVITRIFICATION AND REMELTING OF

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11400	C-V MEASUREMENTS ,SOME PITFALLS IN FAST RAMP
11227	CTRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCTION HEAT FLOW IN SOLID-STATE DEVICES
11158	CURES ,COMPONENT INFANT-MORTALITY - CAUSES AND
11074	CURRENT HOGGING INJECTION LOGIC - NEW FUNCTIONALLY IC'S
11413	CURRENT HOGGING LOGIC - NEW BIPOLAR LOGIC FOR LSI
11222	CURRENT PULSES ,DEGRADATION OF MONOLITHIC SEMICONDUCTOR DEVICES BY HIGH-AMPLITUDE
11585	CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO
11453	CU-SI AND SILVER CONDUCTORS ,WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN ALUMINUM-COPPERALU
11669	CUSTOM DESIGN ,DOING YOUR OWN THING - CMOS
11170	CUT CHIP AREA BY ONE-THIRD ,FIRST OXIDE ISOLATED CMOS CIRCUITS
11489	CVD BOROSILICATE GLASS-FILMS ,WATER ABSORPTION IN
11641	CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE TRAPPING IN
11233	CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND PART RELIABILITY ,DORMANCY AND POWER ON-OFF
11745	CYCLING OF PLASTIC AND CERAMIC IC'S WITH THERMAL-SHOCK PRECONDITIONING ,EXTENDED TEMPERATURE
11449	CYCLING ON ALUMINUM AND GOLD METAL SYSTEMS ,EFFECTS OF FAST TEMPERATURE
11443	CYCLING ,DEGRADATION OF BONDING WIRES AND SEALING GLASSES WITH EXTENDED THERMAL
11142	DAMAGE IN SILICON ,DEVICE IMPLICATIONS OF ION-IMPLANTATION
11704	DAMAGE TO SOLID-STATE DEVICES ,CONTROL OF ELECTROSTATIC
11161	DATA BANK ,HEWLETT-PACKARD FIELD FAILURE
11512	DATA COMMUNICATIONS ,PRECISION PLL SYSTEM FOR
11145	DATA STORAGE APPLICATIONS ,BUBBLE MEMORY STATUS AND TRENDS IN US-GOVERNMENT
11055	DATA ,COMPUTER-AIDED SYNTHESIS OF IC ELECTRICAL DIAGRAM FROM MASK
11103	DC POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS UNDER CONSTANT AND REVERSED
11491	DECAL AIR ISOLATION ,ISOLATION TECHNIQUES FOR FABRICATING IC'S - DIELECTRIC REFILL TECHNIQUES AND
11652	DECODED MNOS STORAGE ARRAYS IN ESFI MOS TECHNOLOGY ,FULLY
11437	DEFECT SITES AT SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT
11450	DEFECT STUDY ,INDUCED PASSIVATION
11408	DEFECTS IN DIELECTRIC FILMS ,DETECTION AND CHARACTERIZATION OF LOCALIZED
11680	DEFECTS IN SILICON P-N JUNCTIONS ,THERMALLY STIMULATED MEASUREMENTS - CHARACTERIZATION OF
11454	DEFECTS IN SILICON WAFERS ,SCANNED SURFACE PHOTOVOLTAGE DETECTION OF
11451	DEFECTS ,ANALYSIS OF DEPOSITED GLASS LAYER
11417	DEFORMATION OCCURING DURING DEPOSITION OF POLYSILICON FILMS
11625	DEFORMATION PROPERTIES OF GOLD THERMOCOMPRESSION BONDING ,HIGH-TEMPERATURE
11661	DEGRADATION CHARACTERISTICS AND MECHANISMS OF OPTICALLY-COUPLED ISOLATOR
11719	DEGRADATION IN OPTICALLY-COUPLED ISOLATOR ,MECHANISMS OF
11435	DEGRADATION MECHANISMS IN REWRITABLE N-CHANNEL FAMOS
11434	DEGRADATION MECHANISMS ,P-CHANNEL REWRITABLE AVALANCHE INJECTION DEVICE OPERATION AND
11443	DEGRADATION OF BONDING WIRES AND SEALING GLASSES WITH EXTENDED THERMAL CYCLING
11222	DEGRADATION OF MONOLITHIC SEMICONDUCTOR DEVICES BY HIGH-AMPLITUDE CURRENT PULSES
11444	DEGRADATION ,SUSCEPTIBILITY OF MICROWELDS IN HYBRID MICROCIRCUITS TO CORROSION
11732	DELAMINATIONS AND VOIDS ,NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC CHIP CAPACITORS FOR
11068	DELAY LINE ARCHITECTURE ,RAZORBACK CCD - HIGH-PERFORMANCE PARALLEL INPUT
11066	DELAY LINE ,MULTIPLEXED VIDEO BANDWIDTH CCD
11253	DEMANDS OF ELECTRONIC DESIGN ,THERMAL
11303	DENSE MEMORIES ,ISOLATION METHOD SHRINKS BIPOLAR CELLS FOR FAST
11304	DENSER BIPOLAR ,COMING UP FAST FROM BEHIND -
11487	DENSITIES OF SURFACE STATES AT SILICON SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF LOW
11521	DENSITY ION-IMPLANTED CMOS TECHNOLOGY ,CMOS-III - HIGH
11194	DEPARTMENT SEMICONDUCTOR PRESENTATION ,GENERAL ELECTRIC AEROSPACE ELECTRONIC SYSTEMS
11453	DEPENDENCE OF ELECTROMIGRATION LIFE IN ALUMINUM-COPPER AL-CU-SI AND SILVER CONDUCTORS ,WIDTH
11268	DEPENDENCE OF FREE CHARGE-TRANSFER IN CCD'S ,STRUCTURE
11651	DEPENDENCE OF SILICON-NITRIDE FILM THICKNESS ON BIPOLAR TRANSISTOR CHARACTERISTICS
11064	DEPLETION MOS TRANSISTORS ,HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT
11322	DEPLETION-MODE FET'S AND BULK-TRANSFER CCD'S ,MEASUREMENTS ON
11451	DEPOSITED GLASS LAYER DEFECTS ,ANALYSIS OF
11277	DEPOSITED SILICON DEVICES ON FUSED SILICA SUBSTRATES ,VACUUM
11417	DEPOSITION OF POLYSILICON FILMS ,DEFORMATION OCCURING DURING
11544	DEPTH PROFILING OF MICROELECTRONIC MATERIALS ,PROBLEMS IN USING SURFACE ANALYSIS TECHNIQUES FOR
11370	DESIGNER ,ION-IMPLANTATION OFFERS FLEXIBILITY TO
11657	DESIGNERS GUIDE FOR LSI
11298	DESORPTION OF GASES FROM PHOTORESIST ,SURFACE
11607	DESPOSITION WEIGHT - POWERFUL CONTROL TOOL FOR THICK-FILM PROCESS
11408	DETECTION AND CHARACTERIZATION OF LOCALIZED DEFECTS IN DIELECTRIC FILMS
11241	DETECTION AND CORRECTION OF MATERIALS AND PROCESSES PROBLEMS IN THIN-FILM NETWORKS
11454	DETECTION OF DEFECTS IN SILICON WAFERS ,SCANNED SURFACE PHOTOVOLTAGE
11541	DETERMINATION OF SURFACE POTENTIALS ON IC'S AT HIGH-FREQUENCIES WITH SEM ,QUANTITATIVE
11574	DETERMINATION OF THICK-FILM CONDUCTOR RESISTOR SYSTEM USEFUL TO 6-GHZ ,PRATICAL ASPECTS IN

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11465	DETERMINATION OF USEFUL LIFE OF 2-LAYER METAILIZATION SYSTEMS VIA ACCELERATED STRESSING
11437	DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE SILICON INTERFACES AS
11090	DEVITRIFICATION AND REMELTING OF CRYSTALS IN GLASS ,FORMATION OF BUBBLES DURING
11379	DIAGNOSTIC TESTING OF MOS RAM'S
11055	DIAGRAM FROM MASK DATA ,COMPUTER-AIDED SYNTHESIS OF IC ELECTRICAL
11475	DIAMOND LABORATORIES ,BOND IMPROVEMENT PROGRAM FOR HARRY
11138	DIAMOND - NEW APPROACH TO MICROELECTRONIC CIRCUIT DESIGN
11436	DIELECTRIC BREAKDOWN OF THERMALLY GROWN SILICON-DIOXIDE BY SELF-QUENCHING TECHNIQUE ,STUDY OF
11736	DIELECTRIC CHARGE STORAGE NON-VOLATILE MEMORY CELLS ,DUAL
11236	DIELECTRIC CONSTANT ,THICK-FILM WITH HIGH
11408	DIELECTRIC FILMS ,DETECTION AND CHARACTERIZATION OF LOCALIZED DEFECTS IN
11629	DIELECTRIC ISOLATION OF SILICON REGIONS
11649	DIELECTRIC ISOLATION ,MINIMIZATION OF PARASITICS IN IC'S BY
11581	DIELECTRIC PROCESS ,SEMICONDUCTOR THERMOPLASTIC
11480	DIELECTRIC QUALITY EVALUATING SYSTEM ,AUTOMATIC
11491	DIELECTRIC REFILL TECHNIQUES AND DECAL AIR ISOLATION ,ISOLATION TECHNIQUES FOR FABRICATING IC'S -
11427	DIELECTRIC RELIABILITY OF SILICON-DIOXIDE FILMS WITH POLYSILICON ELECTRODES ,IMPROVED
11195	DIELECTRICS OF MSI AND LSI DEVICES ,CHARGE TRANSPORT AND POLARIZATION EFFECTS IN
11134	DIELECTRICS ,RADIATION RESISTANCE OF CMOS CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE GATE
11069	DIFFERENTIAL ANALOG CCD FOR TIME SHARED RECURSIVE FILTERS ,DUAL
11567	DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND
11397	DIFFUSION ISOLATED TRANSISTORS FOR LOW-POWER IC'S ,BASE
11064	DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION MOS TRANSISTORS ,HIGH-SPEED LOGIC LSI USING
11354	DIFFUSION SOURCES ,PLANER
11547	DIFUSSED GATE STRUCTURE ,5000-CHANNEL POWER FET WITH NEW
11123	DIGEST OF PAPERS ,GOVERNMENT MICROCIRCUIT APPLICATIONS
11359	DIGEST OF TECHNICAL PAPERS ,1973 SYMPOSIUM ON SEMICONDUCTOR MEMORY TESTING -
11518	DIGEST OF TECHNICAL PAPERS ,1975 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE
11674	DIGITAL AND ANALOG APPLICATIONS ,CMOS PLL - VERSATILE BUILDING BLOCK FOR MICRO-POWER
11644	DIGITAL CIRCUITS ,INFRARED SIGNATURES FOR ANALYSIS OF
11126	DIGITAL COMPUTER ,UNIVERSAL PACKAGING SYSTEM AS APPLIED TO ALL APPLICATIONS
11627	DIGITAL DEVICES ,AUTOMATIC TESTING OF INCOMING
11671	DIGITAL DISPLAYS ,LIQUID CRYSTALS AND CMOS OFFER MINIMAL POWER
11131	DIGITAL IC FAMILY ,RADIATION CHARACTERISTICS OF HARDENED
11132	DIGITAL IC'S ,UNIVERSAL
11663	DIGITAL LOGIC ,MOS - RCA PIONEERED TECHNOLOGY CMOS - RCA'S THRUST IN
11483	DIODE ,CONTACT-HOLE OPENING FOR FABRICATING SCHOTTKY-BARRIER
11399	DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF SODIUM FROM SILICON
11484	DIRECTION OF ELECTROMIGRATION IN GOLD THIN-FILMS ,ON
11264	DIRECTION WITH IIL ,BIPOLAR LSI TAKES NEW
11744	DISCHARGE EFFECTS IN POLYMER ENCAPSULANTS ,THERMALLY STIMULATED
11067	DISCRETE ANALOG SIGNAL PROCESSING ,REPROGRAMMABLE FILTER BANK USING CCD
11329	DISCRETE COMPONENT CHIP MOUNTING TECHNOLOGY FOR HYBRIDS ,INVESTIGATION OF
11563	DISIPATION ,LIFE TEST OF EBS-DIODE AT 200-300-WATT
11291	DISLOCATIONS ON PROPERTIES OF METAL SILICON-DIOXIDE CAPACITORS ,EFFECTS OF
11612	DISPLAY AND DRIVE CIRCUIT PACKAGING ,INTEGRAL LED
11671	DISPLAYS ,LIQUID CRYSTALS AND CMOS OFFER MINIMAL POWER DIGITAL
11638	DISPOSITION OF GALLIUM-PHOSPHIDE HIGH-EFFICIENCY YELLOW SOLID-STATE LAMPS ,VAPOR
11062	DISSIPATION ,DOUBLE IMPLANTED BIPOLAR HIGH-SPEED GATES WITH LOW-POWER
11046	DISTRIBUTED FLOATING-GATE AMPLIFIER IN CCD'S
11564	DMOS PROCESS FOR LSI ,COMPLEMENTARY
11669	DOING YOUR OWN THING - CMOS CUSTOM DESIGN
11297	DOMAIN METHODS TO IC SUSCEPTIBILITY ,APPLICATION OF TIME
11679	DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH
11452	DOPED SILICON BUTTINGCONTACTS ,FAILURE MECHANISM OF METAL-POLYSILICON
11269	DOPED WITH OXYGEN IMPROVES DEVICES ,POLYSILICON LAYER
11233	DORMANCY AND POWER ON-OFF CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND PART RELIABILITY
11688	DOUBLE BEAM IC SOCKET ,LOW PROFILE
11312	DOUBLE EPITAXIAL ISOLATION METHOD FOR FABRICATION OF IC TRANSISTORS
11062	DOUBLE IMPLANTED BIPOLAR HIGH-SPEED GATES WITH LOW-POWER DISSIPATION
11562	DOUBLED HETEROSTRUCTURE LED'S FOR OPTICAL COMMUNICATIONS ,HIGH-POWER LONG-LIVED
11498	DOUBLET COMPRESSION TECHNIQUES ,FAST-SETTLING MONOLITHIC OP-AMP USING
11546	DRAIN ELECTRODE AND MESHED GATE STRUCTURE ,HIGH-POWER MOS FET WITH VERTICAL
11282	DRAIN VOLTAGE LIMITATIONS OF MOS TRANSISTORS
11259	DRAIN-SOURCE PROTECTED MNOS MEMORY DEVICE
11612	DRIVE CIRCUIT PACKAGING ,INTEGRAL LED DISPLAY AND
11137	DRIVER FOR PHASED ARRAY RADAR APPLICATIONS ,HYBRID INTEGRATED FERRITE PHASE-SHIFTER
11409	D/A-CONVERTER ,COMPUTER-AIDED VULNERABILITY ANALYSIS OF
11050	D/A-CONVERTER ,IC 12-BIT
11736	DUAL DIELECTRIC CHARGE STORAGE NON-VOLATILE MEMORY CELLS
11069	DUAL DIFFERENTIAL ANALOG CCD FOR TIME SHARED RECURSIVE FILTERS
11516	DUAL RAMP A/D-CONVERTERS ,APPLICATIONS OF

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11417	DURING DEPOSITION OF POLYSILICON FILMS ,DEFORMATION OCCURING
11090	DURING DEVITRIFICATION AND REMELTING OF CRYSTALS IN GLASS ,FORMATION OF BUBBLES
11741	DYNAMIC PERMEABILITY METHOD FOR EPOXY ENCAPSULATION COMPOUNDS
11542	DYNAMIC RAM USING SEM STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR
11563	EBS-DIODE AT 200-300-WATT DISSIPATION ,LIFE TEST OF
11514	ECL AND TTL RAM TESTING ,BIPOLAR
11276	ECL CIRCUITS ,FEEDTHROUGH IN
11057	ECL COMPATIBLE RAM ,4096-BIT HIGH-SPEED
11058	ECL PROM WITH 15-NS ACCESS ,1024-BIT
11678	ECOM LSI RADIAC COUNTER CIRCUIT ,NUCLEAR RADIATION EFFECTS ON RCA
11439	EDGE PROFILES FOLLOWING OXIDATION ,SOS ISLAND
11476	EFFECTIVE MICROCIRCUIT SCREENING METHODS ,EVALUATION OF HIGH-TEMPERATURE ACCELERATED LIFE TEST TECHNIQUES AS
11160	EFFECTIVENESS ,SCREENING PROGRAM
11610	EFFICIENT HYBRID PACKAGING ,COMPLEX BEAM-LEADED LOGIC AND MEMORY ARRAYS FOR
11367	EFFICIENT TESTING OF COMBINATIONAL LOGIC CELLS IN LARGE-SCALE ARRAYS
11321	ELASTORESISTANCE OF N-TYPE SOS
11194	ELECTRIC AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR PRESENTATION ,GENERAL
11546	ELECTRODE AND MESHED GATE STRUCTURE ,HIGH-POWER MOS FET WITH VERTICAL DRAIN
11049	ELECTRODE CID IMAGER ARRAY ,TRANSPARENT METAL OXIDE
11427	ELECTRODES ,IMPROVED DIELECTRIC RELIABILITY OF SILICON-DIOXIDE FILMS WITH POLYSILICON
11520	ELECTROMAGNETIC RADIATION SCREENING OF MICROCIRCUITS FOR LONG LIFE APPLICATIONS
11103	ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS UNDER CONSTANT AND REVERSED DC POWERING
11448	ELECTROMIGRATION FAILURE IN GOLD THIN-FILM CONDUCTORS
11713	ELECTROMIGRATION FAILURE IN NICHROME THIN-FILM STRIPES
11349	ELECTROMIGRATION FAILURE STUDIES ,PRACTICAL PROBLEMS IN APPLICATION OF ALUMINUM
11484	ELECTROMIGRATION IN GOLD THIN-FILMS ,ON DIRECTION OF
11453	ELECTROMIGRATION LIFE IN ALUMINUM-COPPER AL-CU-SI AND SILVER CONDUCTORS ,WIDTH DEPENDENCE OF
11478	ELECTROMIGRATION RESISTANCE ,COATING NARROW RESISTIVE LINES TO INCREASE
11419	ELECTRONICS WITH PARTICULAR REFERENCE TO COST AND RELIABILITY-VOL-I,STUDY OF MILITARY
11300	ELECTRONS IN N-TYPE INVERSION LAYERS IN -100-SURFACES OF SILICON ,TRANSPORT PROPERTIES OF CONDUCTION
11704	ELECTROSTATIC DAMAGE TO SOLID-STATE DEVICES ,CONTROL OF
11250	ELEMENTS OF SEMICONDUCTOR-DEVICE RELIABILITY
11739	ELEMENTS ,ELECTRICALLY SHORTED SEMICONDUCTOR JUNCTIONS UTILIZED AS PROM
11731	EMISSION AS NON-DESTRUCTIVE TEST FOR BEAM-LEAD BOND INTEGRITY ,USE OF ACOUSTIC
11560	EMITTER COLLECTOR SHORTS IN BIPOLAR DEVICES
11494	EMP HARDENED CMOS CIRCUITS
11389	EMULSION MASK PROCESSING TECHNIQUES
11598	ENCAPSULANTS IN SEMICONDUCTOR APPLICATIONS ,PERFORMANCE OF LIQUID EPOXY
11744	ENCAPSULANTS ,THERMALLY STIMULATED DISCHARGE EFFECTS IN POLYMER
11191	ENCAPSULATED MICROCIRCUITS FOR LONG LIFE APPLICATIONS ,STUDY OF SOLID
11742	ENCAPSULATED MOS DEVICES ,STUDY OF PARASITIC MOS FORMATION MECHANISM IN PLASTIC
11741	ENCAPSULATION COMPOUNDS ,DYNAMIC PERMEABILITY METHOD FOR EPOXY
11127	ENERGY PULSES ON HYBRID CIRCUIT MATERIALS ,EFFECTS OF HIGH
11064	ENHANCEMENT DEPLETION MOS TRANSISTORS ,HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED
11670	ENVIRONMENT ,CMOS IC'S IN AUTOMOBILE
11481	ENVIRONMENTAL FILTER
11312	EPITAXIAL ISOLATION METHOD FOR FABRICATION OF IC TRANSISTORS ,DOUBLE
11650	EPITAXIAL PROCESSING OF SILICON IC'S ,MANUFACTURING METHODS TECHNIQUES AND AUTOMATED CONTROLS FOR CONTINUOUS
11597	EPOXIES FOR HIGH-VOLUME PRODUCTION OF MICROELECTRONIC COMPONENTS ,USE OF
11357	EPOXIES ,BOND CHIPS WITH CONDUCTIVE
11457	EPOXY COMPONENT ATTACH FOR HYBRID FABRICATION ,MULTILEVEL SUBSTRATE TECHNOLOGY AND
11598	EPOXY ENCAPSULANTS IN SEMICONDUCTOR APPLICATIONS ,PERFORMANCE OF LIQUID
11741	EPOXY ENCAPSULATION COMPOUNDS ,DYNAMIC PERMEABILITY METHOD FOR
11593	EPOXY PERFORMANCE TESTING AND NEED FOR STANDARDIZED FORMULATIONS ,CASE FOR BETTER
11596	EPOXY TECHNIQUES FOR HYBRID MICROWAVE IC'S
11149	EPOXY VS EUTECTIC BONDING - STICKY QUESTION
11582	EPOXY-FIBER GLASS SUBSTRATES ,FABRICATION ASSEMBLY AND TEST OF HYBRIDS ON
11232	EQUILIBRATION METHOD OF SETTING CHARGE IN CCD'S ,SURFACE POTENTIAL
11233	EQUIPMENT AND PART RELIABILITY ,DORMANCY AND POWER ON-OFF CYCLING EFFECTS ON ELECTRONIC
11666	EQUIPMENT DESIGN ,CMOS SIMPLIFIES
11634	EQUIPMENT REVIEW - BONDING
11652	ESFI MOS TECHNOLOGY ,FULLY DECODED NMOS STORAGE ARRAYS IN
11583	ESSENTIAL TOOL FOR THICK-FILM PRINTING ,SCREEN -
11549	ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS ,SIMPLE
11392	ETCH SYSTEM FOR IC MANUFACTURE ,AUTOMATED METAL
11538	ETCHING FOR SEMICONDUCTOR APPLICATIONS ,CHARACTERIZATION OF PLASMA
11149	EUTECTIC BONDING - STICKY QUESTION ,EPOXY VS
11139	EVAPORATED ALUMINUM CANTILEVERED BEAMS ,FLEXIBLE MULTILAYER INTERCONNECTION USING
11279	EXCESS NOISE MEASUREMENTS IN ION-IMPLANTED SILICON
11685	EXPERIENCE AND FUTURE PREDICTIONS ,MOS LSI FOR AEROSPACE COMPUTERS - PAST RELIABILITY
11101	EXPERIENCE ,PROM
11063	EXPERIMENTAL AND THEORETICAL STUDY ,NMOS
11327	EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI GE AND SI-GE ,SOME PRATICAL REMARKS ON ''ION OF
11499	EXPERIMENT[illegible]''CATION OF CCD CONCEPT

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11327 EXPITAXIAL GROWTH OF SI GE AND SI-GE ,SOME PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR
11745 EXTENDED TEMPERATURE CYCLING OF PLASTIC AND CERAMIC IC'S WITH THERMAL-SHOCK PRECONDITIONING
11443 EXTENDED THERMAL CYCLING ,DEGRADATION OF BONDING WIRES AND SEALING GLASSES WITH
11440 EXTERNAL PRESSURE - FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK LIDS UNDER
11320 EXTRINSIC SEMICONDUCTOR FILMS ,EFFECT OF SURFACE REGIONS ON ELECTRICAL CONDUCTIVITY OF
11567 FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS
11491 FABRICATING IC'S - DIELECTRIC REFILL TECHNIQUES AND DECAL AIR ISOLATION ,ISOLATION TECHNIQUES FOR
11483 FABRICATING SCHOTTKY-BARRIER DIODE ,CONTACT-HOLE OPENING FOR
11550 FABRICATION AND PERFORMANCE OF ION-IMPLANTED I2L DEVICES
11582 FABRICATION ASSEMBLY AND TEST OF HYBRIDS ON EPOXY-FIBER GLASS SUBSTRATES
11080 FABRICATION BY ION-BEAM SPUTTERING ,HIGH-RESOLUTION
11430 FABRICATION OF BUBBLE MEMORY CHIPS
11312 FABRICATION OF IC TRANSISTORS ,DOUBLE EPITAXIAL ISOLATION METHOD FOR
11097 FABRICATION OF MICROWAVE IC'S ,BEAM TECHNIQUES FOR
11496 FABRICATION OF RADIATION HARDENED MOS DEVICES AND IC'S ,INVESTIGATION OF SOS PROCESSES FOR
11203 FABRICATION OF VIDEO PROTOTYPE MACHINE
11302 FABRICATION SUPPORT FOR THICK-FILM MICROELECTRONICS AND PRINTED WIRING BOARDS ,TECHNOLOGY AND
11577 FABRICATION USING CIRCUIT LAYOUT ,SOLDER BUMP FLIP-CHIP
11457 FABRICATION ,MULTILEVEL SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT ATTACH FOR HYBRID
11239 FACE-DOWN BONDING OF HYBRID COMPONENTS ,PREPARATION OF SUBSTRATES WITH BUMPS FOR
11477 FACTORS AFFECTING AVALANCHE INJECTION INTO INSULATING LAYERS FROM SEMICONDUCTOR SURFACE
11223 FACTS AND FALLACIES OF RADIATION HARD DEVICE SPECS
11219 FACTS ,BEAM-LEADS - WHAT ARE
11353 FAILURE ANALYSIS AND PROCESS ,MICROCIRCUIT MANUFACTURING CONTROL HANDBOOK - GUIDE TO
11231 FAILURE ANALYSIS OF ELECTRONIC PARTS - LABORATORY METHODS
11380 FAILURE ANALYSIS ,APPLICATION OF NEW METHODS AND TECHNIQUES FOR
11648 FAILURE ANALYSIS ,USE OF ION MICROPROBE IN SEMICONDUCTOR
11161 FAILURE DATA BANK ,HEWLETT-PACKARD FIELD
11103 FAILURE IN ALUMINUM THIN-FILMS UNDER CONSTANT AND REVERSED DC POWERING ,ELECTROMIGRATION
11448 FAILURE IN GOLD THIN-FILM CONDUCTORS ,ELECTROMIGRATION
11713 FAILURE IN NICHROME THIN-FILM STRIPES ,ELECTROMIGRATION
11452 FAILURE MECHANISM OF METAL-POLYSILICON DOPED SILICON BUTTINGCONTACTS
11447 FAILURE MECHANISM ,MIGRATORY GOLD RESISTANCE SHORTS - CHEMICAL ASPECTS OF
11385 FAILURE MECHANISMS IN GOLD METALIZED SEALED JUNCTION
11721 FAILURE OF JUNCTION ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED INVERSION
11349 FAILURE STUDIES ,PRACTICAL PROBLEMS IN APPLICATION OF ALUMINUM ELECTROMIGRATION
11729 FAILURES OF ALUMINUM WIRES BONDED TO GOLD METALLIZATION IN MICROSUBSTRATES ,INVESTIGATION INTO
11223 FALLACIES OF RADIATION HARD DEVICE SPECS ,FACTS AND
11131 FAMILY ,RADIATION CHARACTERISTICS OF HARDENED DIGITAL IC
11738 FAMOS PROM RELIABILITY STUDIES
11435 FAMOS ,DEGRADATION MECHANISMS IN REWRITABLE N-CHANNEL
11498 FAST-SETTLING MONOLITHIC OP-AMP USING DOUBLET COMPRESSION TECHNIQUES
11276 FEEDTHROUGH IN ECL CIRCUITS
11137 FERRITE PHASE-SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS ,HYBRID INTEGRATED
11555 FET DEVICES ,CHARGED-COUPLED
11515 FET INPUT OP-AMP ,NEW MONOLITHIC HIGH-PERFORMANCE
11414 FET OP-AMP SPECS ,BEWARE THOSE
11547 FET WITH NEW DIFUSSED GATE STRUCTURE ,5000-CHANNEL POWER
11546 FET WITH VERTICAL DRAIN ELECTRODE AND MESHED GATE STRUCTURE ,HIGH-POWER MOS
11254 FET ,STUDY OF CHARGE STORAGE BEHAVIOR IN METAL ALUMINA SILICON-DIOXIDE SILICON
11322 FET'S AND BULK-TRANSFER CCD'S ,MEASUREMENTS ON DEPLETION-MODE
11537 FET'S ,RECENT ADVANCES IN HIGH-FREQUENCY
11079 FET'S ,STATIC RAM WITH NORMALLY-OFF-TYPE SCHOTTKY BARRIER
11561 FIBER OPTICAL COMMUNICATIONS ,RELIABILITY SEMICONDUCTOR LIGHT SOURCES FOR
11407 FIELD AMPLIFIER ,DEVELOPMENT OF HIGH RELIABILITY RF KEYED CROSSED
11556 FIELD CONTROLLED THYRISTOR - NEW COMPONENT
11161 FIELD FAILURE DATA BANK ,HEWLETT-PACKARD
11510 FIELD PROGRAMMABLE LOGIC ARRAY
11701 FILM CARRIER APPROACHES TO HIGH-VOLUME IC PRODUCTION
11655 FILM METALLIZING FOR CERAMICS ,COMPOSITE
11458 FILM RESISTORS FOR HYBRID MICROCIRCUITS ,PACKAGES AND
11651 FILM THICKNESS ON BIPOLAR TRANSISTOR CHARACTERISTICS ,DEPENDENCE OF SILICON-NITRIDE
11399 FILMS BY FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF SODIUM FROM SILICON DIOXIDE
11641 FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE TRAPPING IN CVD-ALUMINA
11427 FILMS WITH POLYSILICON ELECTRODES ,IMPROVED DIELECTRIC RELIABILITY OF SILICON-DIOXIDE
11622 FILMS ,ATTENUATED TOTAL INFRARED INTERNAL REFLECTION FOR CHARACTERIZATION OF ELECTRONIC
11417 FILMS ,DEFORMATION OCCURING DURING DEPOSITION OF POLYSILICON
11408 FILMS ,DETECTION AND CHARACTERIZATION OF LOCALIZED DEFECTS IN DIELECTRIC

RAC LIBRARY DOCUMENT TITLE — KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11320 FILMS ,EFFECT OF SURFACE REGIONS ON ELECTRICAL CONDUCTIVITY OF EXTRINSIC SEMICONDUCTOR
11656 FILMS ,PHYSICAL PROPERTIES OF THICK SPUTTER-DEPOSITED GLASS
11067 FILTER BANK USING CCD DISCRETE ANALOG SIGNAL PROCESSING ,REPROGRAMMABLE
11481 FILTER ,ENVIRONMENTAL
11069 FILTERS ,DUAL DIFFERENTIAL ANALOG CCD FOR TIME SHARED RECURSIVE
11228 FINAL PRESEAL VISUAL INSPECTION ,TECHNIQUES OF
11587 FINE-LINE SCREEN PRINTING YIELDS AS FUNCTION OF PHYSICAL DESIGN PARAMETERS
11358 FINISHES FOR MICROCIRCUIT PACKAGES ,EVALUATION OF LEAD
11170 FIRST OXIDE ISOLATED CMOS CIRCUITS CUT CHIP AREA BY ONE-THIRD
11440 FLAT-PACK LIDS UNDER EXTERNAL PRESSURE - FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR
11602 FLEXIBILITY OF GLASS WALLED MICROELECTRONICS PACKAGES ,DESIGN OF
11370 FLEXIBILITY TO DESIGNER ,ION-IMPLANTATION OFFERS
11139 FLEXIBLE MULTILAYER INTERCONNECTION USING EVAPORATED ALUMINUM CANTILEVERED BEAMS
11577 FLIP-CHIP FABRICATION USING CIRCUIT LAYOUT ,SOLDER BUMP
11578 FLIP-CHIPS ,SEMICONDUCTOR CHIP ATTACHMENT WITH SMALL BUMP
11071 FLIP-FLOP AND LOGIC GATE WITH JOSEPHSON JUNCTIONS
11473 FLOATING GATE AMPLIFIER ,DESIGN AND OPERATION OF
11046 FLOATING-GATE AMPLIFIER IN CCD'S ,DISTRIBUTED
11227 FLOW IN SOLID-STATE DEVICES ,CTRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCT ON HEAT
11412 FOCUS ON IC ANALOG SWITCHES AND MULTIPLEXERS
11439 FOLLOWING OXIDATION ,SOS ISLAND EDGE PROFILES
11355 FORECAST ,SOS IC TECHNOLOGY
11742 FORMATION MECHANISM IN PLASTIC ENCAPSULATED MOS DEVICES ,STUDY OF PARASITIC MOS
11090 FORMATION OF BUBBLES DURING DEVITRIFICATION AND REMELTING OF CRYSTALS IN GLASS
11399 FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF SODIUM FROM SILICON DIOXIDE FILMS BY
11440 FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK LIDS UNDER EXTERNAL PRESSURE -
11593 FORMULATIONS ,CASE FOR BETTER EPOXY PERFORMANCE TESTING AND NEED FOR STANDARDIZED
11585 FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY
11268 FREE CHARGE-TRANSFER IN CCD'S ,STRUCTURE DEPENDENCE OF
11136 FREQUENCY AMPLIFIER-LIMITER, INTEGRATED INTERMEDIATE
11522 FREQUENCY RESPONSE AND SETTLING TIME OF OP-AMPS ,RELATIONSHIP BETWEEN
11492 FREQUENCY RESPONSES ,MEASUREMENT OF CHARGE RESIDUAL FOR CCD TRANSFER USING IMPULSE AND
11570 FRITLESS METALIZATION ,CHARACTERIZATION OF THICK-FILM
11601 FRUSTRATIONS OF LOW COST PACKAGING AS SEEN BY HYBRID CIRCUIT MANUFACTURER
11652 FULLY DECODED MNOS STORAGE ARRAYS IN ESFI MOS TECHNOLOGY
11543 FUNCTION OF ACTIVE CIRCUIT AREA ,USE OF POWER TRANSFORMATION TO MODEL YIELD OF IC'S AS
11587 FUNCTION OF PHYSICAL DESIGN PARAMETERS ,FINE-LINE SCREEN PRINTING YIELDS AS
11613 FUNCTIONAL HYBRID MICROCIRCUITS ,ACTIVE LASER-TRIMMER FOR PRODUCTION TRIMMING OF
11074 FUNCTIONALLY IC'S ,CURRENT HOGGING INJECTION LOGIC - NEW
11060 FUNDAMENTAL PERFORMANCE LIMITS OF MOS IC'S
11737 FUSE RELIABILITY ,POLYSILICON
11277 FUSED SILICA SUBSTRATES ,VACUUM DEPOSITED SILICON DEVICES ON
11676 FUSIBILE-LINK USED IN PROM'S ,RELIABILITY OF NICHROME
11733 FUSING MECHANISM OF NICHROME RESISTOR LINKS IN PROM'S
11734 FUSING MECHANISMS OF NICHROME THIN-FILMS
11685 FUTURE PREDICTIONS ,MOS LSI FOR AEROSPACE COMPUTERS - PAST RELIABILITY EXPERIENCE AND
11423 FUTURE SATELLITIES ,USE OF IC'S IN
11273 FUTURE ,IIL - PRESENT AND
11470 GAIN OF ION-IMPLANTED TRANSISTORS ,REDUCED
11709 GALLIUM-ARSENIDE ,INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN
11638 GALLIUM-PHOSPHIDE HIGH-EFFICIENCY YELLOW SOLID-STATE LAMPS ,VAPOR DISPOSITION OF
11298 GASES FROM PHOTORESIST ,SURFACE DESORPTION OF
11473 GATE AMPLIFIER ,DESIGN AND OPERATION OF FLOATING
11134 GATE DIELECTRICS ,RADIATION RESISTANCE OF CMOS CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE
11435 GATE OXIDE TRAPS ,TUNNEL INJECTION INTO
11547 GATE STRUCTURE ,5000-CHANNEL POWER FET WITH NEW DIFUSSED
11546 GATE STRUCTURE ,HIGH-POWER MOS FET WITH VERTICAL DRAIN ELECTRODE AND MESHED
11071 GATE WITH JOSEPHSON JUNCTIONS ,FLIP-FLOP AND LOGIC
11133 GATED VIDEO AMPLIFIER ,RADIATION TOLERANT
11679 GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON
11062 GATES WITH LOW-POWER DISSIPATION ,DOUBLE IMPLANTED BIPOLAR HIGH-SPEED
11327 GE AND SI-GE ,SOME PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI
11154 GENERAL ELECTRIC AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR PRESENTATION
11128 GENERAL PURPOSE COMPUTER FOR SATELLITE APPLICATIONS
11296 GENERATED TROUBLESHOOTING TREES - PROGRAM ,COMPUTER
11722 GENERATION AND PARASITIC BIPOLAR ACTION IN IGFET DEVICE ,RELIABILITY IMPLICATIONS OF HOT ELECTRON
11083 GENERATION OF MICROPROCESSORS ,N-CHANNEL MOS TECHNOLOGY YIELDS NEW
11082 GEOMETRY IN SPUTTERING TECHNOLOGY ,NEW
11264 GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT SINKS ,THERMAL PROPERTIES OF ANNULAR AND ARRAY

RAC LIBRARY DOCUMENT TITLE — KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11656 GLASS FILMS ,PHYSICAL PROPERTIES OF THICK SPUTTER-DEPOSITED
11451 GLASS LAYER DEFECTS ,ANALYSIS OF DEPOSITED
11582 GLASS SUBSTRATES ,FABRICATION ASSEMBLY AND TEST OF HYBRIDS ON EPOXY [illegible]
11109 GLASS TECHNOLOGY ,ADVANCES IN SOLDER
11602 GLASS WALLED MICROELECTRONICS PACKAGES ,DESIGN OF FLEXIBILITY OF
11399 GLASS ,COMPLETE REMOVAL OF BORON FROM SILICON-DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE
11090 GLASS ,FORMATION OF BUBBLES DURING DEVITRIFICATION AND REMELTING OF CRYSTALS IN
11572 GLASSES NEW CONCEPT ,HIGH-TEMPERATURE VISCOSITY CONTROL IN MULTILAYER
11443 GLASSES WITH EXTENDED THERMAL CYCLING ,DEGRADATION OF BONDING WIRES AND SEALING
11489 GLASS-FILMS ,WATER ABSORPTION IN CVD BOROSILICATE
11727 GOLD ALUMINUM INTERMETALLICS ON THIN-FILM HYBRID MICROCIRCUIT SUBSTRATES
11700 GOLD CONNECTOR CONTACTS - DEVELOPMENT IN SEARCH FOR ALTERNATE MATERIALS
11449 GOLD METAL SYSTEMS ,EFFECTS OF FAST TEMPERATURE CYCLING ON ALUMINUM AND
11385 GOLD METALIZED SEALED JUNCTION ,FAILURE MECHANISMS IN
11728 GOLD METALLIZATION ,METALLURGICAL ASPECTS OF ALUMINUM WIRE BONDS TO
11636 GOLD ON SILICON POWER-DEVICES ,EFFECTS OF OXYGEN AND
11240 GOLD PLATING - EFFECT OF DESIGN SPECIFICATION
11447 GOLD RESISTANCE SHORTS - CHEMICAL ASPECTS OF FAILURE MECHANISM ,MIGRATORY
11446 GOLD RESISTIVE SHORTS IN MICROCIRCUITS ,MIGRATED
11625 GOLD THERMOCOMPRESSION BONDING ,HIGH-TEMPERATURE DEFORMATION PROPERTIES OF
11448 GOLD THIN-FILM CONDUCTORS ,ELECTROMIGRATION FAILURE IN
11484 GOLD THIN-FILMS ,ON DIRECTION OF ELECTROMIGRATION IN
11140 GOLD WIRES IN HIGH-ACCELERATION HYBRID APPLICATIONS ,I-MIL
11591 GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM
11711 GOLD ,EFFECT OF SURFACE CONTAMINATION ON THERMOCOMPRESSION BONDABILITY OF
11729 GOLD METALLIZATION IN MICROSUBSTRATES ,INVESTIGATION INTO FAILURES OF ALUMINUM WIRES BONDED TO
11698 GOLD-PLATED COPPER LEADS ON THIN-FILM CIRCUITS UNDER ACCELERATED-AGING STRENGTH OF
11123 GOVERNMENT MICROCIRCUIT APPLICATIONS DIGEST OF PAPERS
11436 GROWN SILICON-DIOXIDE BY SELF-QUENCHING TECHNIQUE ,STUDY OF DIELECTRIC [illegible] OF THERMALLY
11425 GROWN SILICON-DIOXIDE SURFACES BY CONTACT ANGLE MEASUREMENTS ,CHARACTERIZATION OF THERMALLY
11327 GROWTH OF SI GE AND SI-GE ,SOME PRACTICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL
11199 GUIDANCE USING LSI ,STRAPDOWN INERTIAL
11657 GUIDE FOR LSI ,DESIGNERS
11353 GUIDE TO FAILURE ANALYSIS AND PROCESS ,MICROCIRCUIT MANUFACTURING CONTROL HANDBOOK -
11105 GUIDE ,HYBRID MICROCIRCUIT DESIGN
11328 GUIDELINES FOR USE OF ADHESIVES AND ORGANIC COATINGS IN HYBRIDS ,DESIGN
11278 HALL EFFECT IN SOS
11353 HANDBOOK - GUIDE TO FAILURE ANALYSIS AND PROCESS ,MICROCIRCUIT MANUFACTURING CONTROL
11223 HARD DEVICE SPECS ,FACTS AND FALLACIES OF RADIATION
11494 HARDENED CMOS CIRCUITS ,EMP
11699 HARDENED CMOS IC'S ,TOTAL-DOSE RADIATION
11131 HARDENED DIGITAL IC FAMILY ,RADIATION CHARACTERISTICS OF
11496 HARDENED MIS DEVICES AND IC'S ,INVESTIGATION OF SOS PROCESSES FOR FABRICATION OF RADIATION
11416 HARDENED MIS IC'S ,INVESTIGATION OF THIN-FILM SILICON PROCESS FOR RADIATION
11206 HARDENED MIS INPUT/OUTPUT SUBSYSTEM DEVELOPMENT ,RADIATION
11375 HARDENED MOS INPUT AND OUTPUT CIRCUITRY-VOL-I
11557 HARDNESS ,CMOS OPTIMIZATION FOR RADIATION
11475 HARRY DIAMOND LABORATORIES ,BOND IMPROVEMENT PROGRAM FOR
11227 HEAT FLOW IN SOLID-STATE DEVICES ,CTRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCTION
11284 HEAT SINKS ,THERMAL PROPERTIES OF ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE
11235 HEATING APPLICATIONS IN MICROCIRCUIT ASSEMBLY ,PREHEATED
11675 HELIUM-NEON LASER ,SILICON SLICE ANALYSER USING
11179 HERMETIC IC'S IN PLASTIC PACKAGES ,RELIABILITY EVALUATION OF
11603 HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE
11600 HERMETICALLY SEALED SEMICONDUCTOR PACKAGES ,MEASUREMENT AND CONTROL OF ATMOSPHERE IN
11124 HERMETICALLY SEALED-IN CONTAMINANTS ,IC PACKAGES AND
11562 HETEROSTRUCTURE LED'S FOR OPTICAL COMMUNICATIONS ,HIGH-POWER LONG-LIVED DOUBLE
11161 HEWLETT-PACKARD FIELD FAILURE DATA BANK
11521 HIGH DENSITY ION-IMPLANTED CMOS TECHNOLOGY ,CMOS-III -
11236 HIGH DIELECTRIC CONSTANT ,THICK-FILM WITH
11127 HIGH ENERGY PULSES ON HYBRID CIRCUIT MATERIALS ,EFFECTS OF
11054 HIGH QUALITY SILICON-DIOXIDE FOR IC'S
11129 HIGH RELIABILITY APPLICATIONS ,DESIGN OF POWER HYBRID MICROCIRCUITS FOR
11407 HIGH RELIABILITY RF KEYED CROSSED FIELD AMPLIFIER ,DEVELOPMENT OF
11590 HIGH RELIABILITY ULTRASONIC WIRE BONDING
11455 HIGH RESOLUTION SYSTEM FOR PHOTORESPONSE MAPPING OF SEMICONDUCTOR DEVICES
11523 HIGH SLEW RATE MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY PNP TRANSISTORS
11497 HIGH-SPEED CMOS/SOS CIRCUITS ,LOW-POWER
11603 HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11262	HIGHLIGHTS - SOLID-STATE TECHNOLOGY
11548	HIGHLY RELIABLE HIGH-VOLTAGE TRANSISTORS
11140	HIGH-ACCELERATION HYBRID APPLICATIONS ,1-MIL GOLD WIRES IN
11222	HIGH-AMPLITUDE CURRENT PULSES ,DEGRADATION OF MONOLITHIC SEMICONDUCTOR DEVICES BY
11626	HIGH-DENSITY MEMORIES ,THERMAL OXIDE ISOLATION PROCESS FOR
11638	HIGH-EFFICIENCY YELLOW SOLID-STATE LAMPS ,VAPOR DISPOSITION OF GALLIUM-PHOSPHIDE
11541	HIGH-FREQUENCIES WITH SEM ,QUANTITATIVE DETERMINATION OF SURFACE POTENTIALS ON IC'S AT
11537	HIGH-FREQUENCY FET'S ,RECENT ADVANCES IN
11515	HIGH-PERFORMANCE FET INPUT OP-AMP ,NEW MONOLITHIC
11068	HIGH-PERFORMANCE PARALLEL INPUT DELAY LINE ARCHITECTURE ,RAZORBACK CCD -
11562	HIGH-POWER LONG-LIVED DOUBLED HETEROSTRUCTURE LED'S FOR OPTICAL COMMUNICATIONS
11546	HIGH-POWER MOS FET WITH VERTICAL DRAIN ELECTRODE AND MESHED GATE STRUCTURE
11684	HIGH-POWER PULSE TESTING OF IC'S
11052	HIGH-PRECISION COMPONENT TOLERANT A/D-CONVERTER
11615	HIGH-RELIABILITY COMPLEX HYBRID IC'S
11620	HIGH-RELIABILITY HYBRID CIRCUITS ,ELECTRICAL SCREEN FOR
11673	HIGH-RELIABILITY TECHNOLOGY ,CMOS IS
11726	HIGH-RELIABILITY THIN-FILM METALIZATION ,BERYLLIUM -
11080	HIGH-RESOLUTION FABRICATION BY ION-BEAM SPUTTERING
11061	HIGH-SENSITIVITY CHARGE-TRANSFER SENSE-AMPLIFIER
11513	HIGH-SPEED ANALOG SWITCH ,APPLICATIONS OF 10-OHM
11047	HIGH-SPEED CLOCK-PULSELESS SCANNER FOR MOS IMAGE SENSORS ,ULTRA
11710	HIGH-SPEED CMOS SOS
11057	HIGH-SPEED ECL COMPATIBLE RAM ,4096-BIT
11062	HIGH-SPEED GATES WITH LOW-POWER DISSIPATION ,DOUBLE IMPLANTED BIPOLAR
11064	HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION MOS TRANSISTORS
11267	HIGH-SPEED P-CHANNEL RANDOM ACCESS 1024-BIT MEMORY MADE WITH ELECTRON LITHOGRAPHY
11366	HIGH-SPEED TTL COMPATIBLE MOS LOGIC ,VMOS -
11476	HIGH-TEMPERATURE ACCELERATED LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING METHODS ,EVALUATION OF
11625	HIGH-TEMPERATURE DEFORMATION PROPERTIES OF GOLD THERMOCOMPRESSION BONDING
11464	HIGH-TEMPERATURE OPERATING TESTS - CONTROL FOR CONTAMINATED MICROCIRCUIT PROCESSES
11572	HIGH-TEMPERATURE VISCOSITY CONTROL IN MULTILAYER GLASSES NEW CONCEPT
11169	HIGH-TEMPERATURES,TESTING IC'S AT
11545	HIGH-VOLTAGE BIPOLAR POWER-TRANSISTOR ,MICROWAVE
11585	HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER
11548	HIGH-VOLTAGE TRANSISTORS ,HIGHLY RELIABLE
11701	HIGH-VOLUME IC PRODUCTION ,FILM CARRIER APPROACHES TO
11597	HIGH-VOLUME PRODUCTION OF MICROELECTRONIC COMPONENTS ,USE OF EPOXIES FOR
11074	HOGGING INJECTION LOGIC - NEW FUNCTIONALLY IC'S ,CURRENT
11413	HOGGING LOGIC - NEW BIPOLAR LOGIC FOR LSI ,CURRENT
11722	HOT ELECTRON GENERATION AND PARASITIC BIPOLAR ACTION IN IGFET DEVICE ,RELIABILITY IMPLICATIONS OF
11603	HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER
11140	HYBRID APPLICATIONS ,1-MIL GOLD WIRES IN HIGH-ACCELERATION
11601	HYBRID CIRCUIT MANUFACTURER ,FRUSTRATIONS OF LOW COST PACKAGING AS SEEN BY
11127	HYBRID CIRCUIT MATERIALS ,EFFECTS OF HIGH ENERGY PULSES ON
11575	HYBRID CIRCUITS - MANUFACTURING PROCESS ,MULTILAYER CERAMIC CAPACITOR CHIPS FOR
11459	HYBRID CIRCUITS - THEIR EFFECT ON RELIABILITY ,REPAIRS TO COMPLEX
11620	HYBRID CIRCUITS ,ELECTRICAL SCREEN FOR HIGH-RELIABILITY
11594	HYBRID CIRCUITS ,SELECTION AND CONTROLS OF POLYMERS USED IN MANUFACTURE OF
11239	HYBRID COMPONENTS ,PREPARATION OF SUBSTRATES WITH BUMPS FOR FACE-DOWN BONDING OF
11611	HYBRID ELECTRONIC WATCH PROTOTYPE ,THICK-FILM
11457	HYBRID FABRICATION ,MULTILEVEL SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT ATTACH FOR
11130	HYBRID IC TECHNOLOGY ,MINIATURIZATION OF TELEVISION CAMERAS THROUGH
11615	HYBRID IC'S ,HIGH-RELIABILITY COMPLEX
11371	HYBRID IC'S ,PRODUCTION ENGINEERING MEASURES AUTOMATIC ASSEMBLY OF
11237	HYBRID IC'S ,THICK-FILM
11135	HYBRID INTEGRATED 40-WATT 2-STAGE AMPLIFIER WITH OCTAVE BANDWIDTH ,UHF
11137	HYBRID INTEGRATED FERRITE PHASE-SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS
11592	HYBRID MICROCIRCUIT BEAM-LEAD DEVICES FOR POSTMORTEM TESTS ,REMOVAL OF
11105	HYBRID MICROCIRCUIT DESIGN GUIDE
11677	HYBRID MICROCIRCUIT SOLDERING TECHNIQUES ,RF
11727	HYBRID MICROCIRCUIT SUBSTRATES ,GOLD ALUMINUM INTERMETALLICS ON THIN-FILM
11376	HYBRID MICROCIRCUIT TECHNOLOGY IN BRITISH NATIONAL SPACE PROGRAM
11287	HYBRID MICROCIRCUITS CONTAINING BEAM-LEAD DEVICES ,DEVELOPMENT OF PROCESSES FOR
11129	HYBRID MICROCIRCUITS FOR HIGH RELIABILITY APPLICATIONS ,DESIGN OF POWER
11444	HYBRID MICROCIRCUITS TO CORROSION DEGRADATION ,SUSCEPTIBILITY OF MICROWELDS IN
11613	HYBRID MICROCIRCUITS ,ACTIVE LASER-TRIMMER FOR PRODUCTION TRIMMING OF FUNCTIONAL
11642	HYBRID MICROCIRCUITS ,APPROACH FOR EVALUATING POLYMER MATERIALS AS PROTECTIVE COATINGS ON
11595	HYBRID MICROCIRCUITS ,CONFORMAL POLYMER COATING FOR NON-LIDDED
11242	HYBRID MICROCIRCUITS ,EFFECTS OF BONDING TECHNIQUES ON RELIABILITY OF
11458	HYBRID MICROCIRCUITS ,PACKAGES AND FILM RESISTORS FOR
11697	HYBRID MICROCIRCUITS ,RIBBON WIRE VERSUS ROUND WIRE RELIABILITY FOR
11098	HYBRID MICROCIRCUITS ,THIN-FILM MULTILAYERING TECHNIQUE FOR
11608	HYBRID MICROELECTRONIC ASSEMBLIES ,SPOT IN-LINE QUALITY CONTROL SYSTEM FOR

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11612	INTEGRAL LED DISPLAY AND DRIVE CIRCUIT PACKAGING
11135	INTEGRATED 45-WATT 2-STAGE AMPLIFIER WITH OCTAVE BANDWIDTH ,UHF HYBRID
11179	IC'S IN PLASTIC PACKAGES ,RELIABILITY EVALUATION OF HERMETIC
11074	IC'S ,CURRENT HOGGING INJECTION LOGIC - NEW FUNCTIONALLY
11708	INTEGRATED DEVICE ANALYSIS MODELING AND DESIGN
11137	INTEGRATED FERRITE PHASE-SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS ,HYBRID
11136	INTEGRATED INTERMEDIATE FREQUENCY AMPLIFIER-LIMITER
11204	INTEGRATED SOLID-STATE TRANSCEIVER
11198	INTEGRATED THERMIONIC CIRCUITS
11275	INTEGRATION PROCESS ,CMOS AND COMPLEMENTARY ISOLATED BIPOLAR TRANSISTOR MONOLITHIC
11619	INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES
11731	INTEGRITY ,USE OF ACOUSTIC EMISSION AS NON-DESTRUCTIVE TEST FOR BEAM-LEAD BOND
11125	INTERCONNECT PACKAGING ,BEAM-LEADED
11374	INTERCONNECTION TECHNIQUE FOR IC AND THEIR APPLICATION TO SPACECRAFT ELECTRONIC SYSTEMS ,MULTILAYER
11139	INTERCONNECTION USING EVAPORATED ALUMINUM CANTILEVERED BEAMS ,FLEXIBLE MULTILAYER
11696	INTERCONNECTIONS ON MICROCIRCUITS ,RELIABILITY ON
11618	INTERCONNECTIONS ,TIME-DEPENDENT RELATIONSHIPS IN SOLAR
11141	INTERCONNECTS FOR MSI AND LSI ,ENGINEERING STUDY OF DEVELOPMENT OF 2-LEVEL ANODIZED ALUMINUM
11679	INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON
11643	INTERFACE PROPERTIES ,EFFECT OF OXYGEN ION IMPLEMENTATION ON SILICON SILICON-DIOXIDE
11487	INTERFACE ,MEASUREMENT OF LOW DENSITIES OF SURFACE STATES AT SILICON SILICON-DIOXIDE
11437	INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE SILICON
11730	INTERFEROMETER FOR ULTRASONIC BONDING STUDIES ,DESIGN AND USE OF LASER
11258	INTERGRATED MONOLITHIC PHOTOSENSOR ARRAYS
11136	INTERMEDIATE FREQUENCY AMPLIFIER-LIMITER,INTEGRATED
11727	INTERMETALLICS ON THIN-FILM HYBRID MICROCIRCUIT SUBSTRATES ,GOLD ALUMINUM
11622	INTERNAL REFLECTION FOR CHARACTERIZATION OF ELECTRONIC FILMS ,ATTENUATED TOTAL INFRARED
11542	INTERNAL WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC RAM USING SEM STROBOSCOPIC TECHNIQUES
11535	INTERNATIONAL ELECTRON DEVICES MEETING 1975
11568	INTERNATIONAL MICROELECTRONIC SYMPOSIUM ,1974
11518	INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS ,1975 IEEE
11456	INTRODUCTION ,TUTORIAL SESSIONS ON HYBRID TECHNOLOGY
11721	INVERSION FAILURE OF JUNCTION ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED
11300	INVERSION LAYERS IN -100-SURFACES OF SILICON ,TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN N-TYPE
11550	ION-IMPLANTED IIL DEVICES ,FABRICATION AND PERFORMANCE OF
11643	ION IMPLEMENTATION ON SILICON SILICON-DIOXIDE INTERFACE PROPERTIES ,EFFECT OF OXYGEN
11648	ION MICROPROBE IN SEMICONDUCTOR FAILURE ANALYSIS ,USE OF
11080	ION-BEAM SPUTTERING ,HIGH-RESOLUTION FABRICATION BY
11142	ION-IMPLANTATION DAMAGE IN SILICON ,DEVICE IMPLICATIONS OF
11370	ION-IMPLANTATION OFFERS FLEXIBILITY TO DESIGNER
11299	ION-IMPLANTATION ,MANUFACTURING METHODS FOR
11418	ION-IMPLANTATIONS,MANUFACTURING METHODS FOR
11521	ION-IMPLANTED CMOS TECHNOLOGY ,CMOS-III - HIGH DENSITY
11271	ION-IMPLANTED MOS CAPACITORS ,NON-EQUILIBRIUM PHENOMENA IN
11279	ION-IMPLANTED SILICON ,EXCESS NOISE MEASUREMENTS IN
11470	ION-IMPLANTED TRANSISTORS ,REDUCED GAIN OF
11270	IRRADIATION EFFECTS IN SILICON-DIOXIDE INSULATED MIS DEVICES ,LOW-TEMPERATURE
11603	IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL
11673	IS HIGH-RELIABILITY TECHNOLOGY ,CMOS
11439	ISLAND EDGE PROFILES FOLLOWING OXIDATION ,SOS
11275	ISOLATED BIPOLAR TRANSISTOR MONOLITHIC INTEGRATION PROCESS ,CMOS AND COMPLEMENTARY
11170	ISOLATED CMOS CIRCUITS CUT CHIP AREA BY ONE-THIRD ,FIRST OXIDE
11721	ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION
11397	ISOLATED TRANSISTORS FOR LOW-POWER IC'S ,BASE DIFFUSION
11637	ISOLATION FOR IC'S ,POLYCRYSTALLINE SILICON
11312	ISOLATION METHOD FOR FABRICATION OF IC TRANSISTORS ,DOUBLE EPITAXIAL
11303	ISOLATION METHOD SHRINKS BIPOLAR CELLS FOR FAST DENSE MEMORIES
11629	ISOLATION OF SILICON REGIONS ,DIELECTRIC
11626	ISOLATION PROCESS FOR HIGH-DENSITY MEMORIES ,THERMAL OXIDE
11567	ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED
11491	ISOLATION TECHNIQUES FOR FABRICATING IC'S - DIELECTRIC REFILL TECHNIQUES AND DECAL AIR ISOLATION
11384	ISOLATION TECHNIQUES ,BIBLIOGRAPHY ON SEMICONDUCTOR DEVICE
11679	ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE
11491	ISOLATION ,ISOLATION TECHNIQUES FOR FABRICATING IC'S - DIELECTRIC REFILL TECHNIQUES AND DECAL AIR
11649	ISOLATION ,MINIMIZATION OF PARASITICS IN IC'S BY DIELECTRIC
11661	ISOLATOR ,DEGRADATION CHARACTERISTICS AND MECHANISMS OF OPTICALLY-COUPLED

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11719 ISOLATOR ,MECHANISMS OF DEGRADATION IN OPTICALLY-COUPLED
11471 IT ALL TOGETHER ,L5 PHYSICAL DESIGN PUTS
11227 ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCTION HEAT FLO.. IN SOLID-STATE DEVICES ,CTRUMP -
11051 JFET BIPOLAR 8-CHANNEL ANALOG MULTIPLEXER
11238 JOINING ,MODULE MATERIALS FOR CONTROLLED COLLAPSE CHIP
11619 JOINTS CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER
11071 JOSEPHSON JUNCTIONS ,FLIP-FLOP AND LOGIC GATE WITH
11293 JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON ,LONG TER.. MEMORY IN
11621 JUNCTION DEVICES ,RELIABILITY OF BEAM-LEAD SEALED
11208 JUNCTION DEVICES ,RELIABILITY STUDY OF BEAM-LEAD SEALED
11721 JUNCTION ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF
11385 JUNCTION ,FAILURE MECHANISMS IN GOLD METALIZED SEALED
11739 JUNCTIONS UTILIZED AS PROM ELEMENTS ,ELECTRICALLY SHORTED SEMICONDUCTOR
11071 JUNCTIONS ,FLIP-FLOP AND LOGIC GATE WITH JOSEPHSON
11549 JUNCTIONS ,SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE I'I PLANE AND PLANAR P-N
11680 JUNCTIONS ,THERMALLY STIMULATED MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN SILICON P-N
11672 KEEPING UP WITH TIMES THROUGH COMPUTER-AIDED DESIGN
11407 KEYED CROSSED FIELD AMPLIFIER ,DEVELOPMENT OF HIGH RELIABILITY RF
11378 KOVAR PACKAGE LEADS ,METALLURGICAL ANALYSIS OF STRESS-CORROSION CRACKING OF
11471 L5 PHYSICAL DESIGN PUTS IT ALL TOGETHER
11475 LABORATORIES ,BOND IMPROVEMENT PROGRAM FOR HARRY DIAMOND
11231 LABORATORY METHODS ,FAILURE ANALYSIS OF ELECTRONIC PARTS -
11638 LAMPS ,VAPOR DISPOSITION OF GALLIUM-PHOSPHIDE HIGH-EFFICIENCY YELLOW SOLID-STATE
11367 LARGE-SCALE ARRAYS ,EFFICIENT TESTING OF COMBINATIONAL LOGIC CELLS IN
11730 LASER INTERFEROMETER FOR ULTRASONIC BONDING STUDIES ,DESIGN AND USE OF
11540 LASER SCANNING OF ACTIVE SEMICONDUCTOR DEVICES
11614 LASER SYSTEM ,METHOD OF OBTAINING OPTIMUM TRIMMING PERFORMANCE FROM
11675 LASER ,SILICON SLICE ANALYSER USING HELIUM-NEON
11613 LASER-TRIMMER FOR PRODUCTION TRIMMING OF FUNCTIONAL HYBRID MICROCIRCUITS ,ACTIVE
11579 LASER-TRIMMING OF THICK-FILM AND THIN-FILM RESISTORS ,DU
11580 LASER-TRIMMING OF THICK-FILM RESISTORS FO MILITARY APPLICATIONS
11631 LASER-TRIMMING ON CHIP
11261 LATCH-UP IN CMOS IC'S
11566 LATERAL THERMAL INSTABILITIES IN POWER-TRANSISTORS,COMPUTER MODEL FOR
11451 LAYER DEFECTS ,ANALYSIS OF DEPOSITED GLASS
11269 LAYER DOPED WITH OXYGEN IMPROVES DEVICES ,POLYSILICON
11653 LAYERS BY X-RAY APPEARANCE POTENTIAL SPECTROSCOPY ,INVESTIGATION OF SURFACE OXIDE
11477 LAYERS FROM SEMICONDUCTOR SURFACE ,FACTORS AFFECTING AVALANCHE INJECTION INTO INSULATING
11370 LAYERS IN <100>SURFACES OF SILICON ,TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN N-TYPE INVERSION
11577 LAYOUT ,SOLDER BUMP FLIP-CHIP FABRICATION USING CIRCUIT
11358 LEAD FINISHES FOR MICROCIRCUIT PACKAGES ,EVALUATION OF
11698 LEADS ON THIN-FILM CIRCUITS UNDER ACCELERATED-AGING,STRENGTH OF GOLD-PLATED COPPER
11619 LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL
11378 LEADS ,METALLURGICAL ANALYSIS OF STRESS-CORROSION CRACKING OF KOVAR PACKAGE
11612 LED DISPLAY AND DRIVE CIRCUIT PACKAGING ,INTEGRAL
11562 LED'S FOR OPTICAL COMMUNICATIONS ,HIGH-POWER LONG-LIVED DOUBLED HETEROSTRUCTURE
11440 LIDS UNDER EXTERNAL PRESSURE - FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK
11520 LIFE APPLICATIONS ,ELECTROMAGNETIC RADIATION SCREENING OF MICROCIRCUITS FOR LONG
11191 LIFE APPLICATIONS ,STUDY OF SOLID ENCAPSULATED MICROCIRCUITS FOR LONG
11453 LIFE IN ALUMINUM-COPPER AL-CU-SI AND SILVER CONDUCTORS ,WIDTH DEPENDENCE OF ELECTROMIGRATION
11465 LIFE OF 2-LAYER METALLIZATION SYSTEMS VIA ACCELERATED STRESSING ,DETERMINATION OF USEFUL
11563 LIFE TEST OF EBS-DIODE AT 200-300-WATT DISSIPATION
11476 LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING METHODS ,EVALUATION OF HIGH-TEMPERATURE ACCELERATED
11692 LIFE ,MICROCIRCUIT PACEMAKER SPACE AGE SPIN-OFF TO ACHIEVE RELIABILITY AND LONG
11561 LIGHT SOURCES FOR FIBER OPTICAL COMMUNICATIONS ,RELIABILITY SEMICONDUCTOR
11060 LIMITS OF MOS IC'S ,FUNDAMENTAL PERFORMANCE
11432 LINE ADDRESSABLE RAM ,CCD
11068 LINE ARCHITECTURE ,RAZORBACK CCD - HIGH-PERFORMANCE PARALLEL INPUT DELAY
11665 LINE COMES OF AGE ,CMOS STANDARD-PARTS
11066 LINE ,MULTIPLEXED VIDEO BANDWIDTH CCD DELAY
11681 LINEAR IC'S ,REWORK OF
11263 LINEARITY OF ELECTRICAL CHARGE-INJECTION INTO CCD'S
11478 LINES TO INCREASE ELECTROMIGRATION RESISTANCE ,OMATING NAPROW RESISTIVE
11733 LINKS IN PROM'S ,FUSING MECHANISM OF NICHROME RESISTOR
11671 LIQUID CRYSTALS AND CMOS OFFER MINIMAL POWER DIGITAL DISPLAYS
11598 LIQUID EPOXY ENCAPSULANTS IN SEMICONDUCTOR APPLICATIONS ,PERFORMANCE OF
11267 LITHOGRAPHY ,HIGH-SPEED P-CHANNEL RANDOM ACCESS 1024-BIT MEMORY MADE WITH ELECTRON
11536 LITHOGRAPHY ,PATHWAYS AND PITFALLS IN DEVICE
11053 LITHOGRAPHY ,POSITIVE OPTICAL

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11408	LOCALIZED DEFECTS IN DIELECTRIC FILMS ,DETECTION AND CHARACTERIZATION OF
11610	LOGIC AND MEMORY ARRAYS FOR EFFICIENT HYBRID PACKAGING ,COMPLEX BEAM-LEADED
11510	LOGIC ARRAY ,FIELD PROGRAMMABLE
11367	LOGIC CELLS IN LARGE-SCALE ARRAYS ,EFFICIENT TESTING OF COMBINATIONAL
11413	LOGIC FOR LSI ,CURRENT HOGGING LOGIC - NEW BIPOLAR
11071	LOGIC GATE WITH JOSEPHSON JUNCTIONS ,FLIP-FLOP AND
11064	LOGIC LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION MOS TRANSISTORS ,HIGH-SPEED
11413	LOGIC - NEW BIPOLAR LOGIC FOR LSI ,CURRENT HOGGING
11074	LOGIC - NEW FUNCTIONALLY IC'S ,CURRENT HOGGING INJECTION
11509	LOGIC TO IMPROVE PERFORMANCE IN CMOS AND MICROPROCESSOR SYSTEMS ,USING BIPOLAR
11663	LOGIC ,MOS - RCA PIONEERED TECHNOLOGY CMOS - RCA'S THRUST IN DIGITAL
11073	LOGIC ,SCHOTTKY TRANSISTOR
11366	LOGIC ,VMOS - HIGH-SPEED TTL COMPATIBLE MOS
11520	LONG LIFE APPLICATIONS ,ELECTROMAGNETIC RADIATION SCREENING OF MICROCIRCUITS FOR
11191	LONG LIFE APPLICATIONS ,STUDY OF SOLID ENCAPSULATED MICROCIRCUITS FOR
11692	LONG LIFE ,MICROCIRCUIT PACEMAKER SPACE AGE SPIN-OFF TO ACHIEVE RELIABILITY AND
11293	LONG TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON
11562	LONG-LIVED DOUBLED HETEROSTRUCTURE LED'S FOR OPTICAL COMMUNICATIONS ,HIGH-POWER
11460	LOOSE PARTICLES AND COATING MATERIALS ,HYBRID TECHNOLOGY
11601	LOW COST PACKAGING AS SEEN BY HYBRID CIRCUIT MANUFACTURER ,FRUSTRATIONS OF
11487	LOW DENSITIES OF SURFACE STATES AT SILICON SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF
11497	LOW-POWER HIGH-SPEED CMOS/SOS CIRCUITS
11688	LOW PROFILE DOUBLE BEAM IC SOCKET
11576	LOW-OHM CHIP RESISTORS ,ULTRA
11143	LOW-POWER CMOS MASS MEMORY
11062	LOW-POWER DISSIPATION ,DOUBLE IMPLANTED BIPOLAR HIGH-SPEED GATES WITH
11397	LOW-POWER IC'S ,BASE DIFFUSION ISOLATED TRANSISTORS FOR
11104	LOW-POWER SCHOTTKY TTL
11270	LOW-TEMPERATURE IRRADIATION EFFECTS IN SILICON-DIOXIDE INSULATED MIS DEVICES
11401	LSI APPLICATIONS ,TUNGSTEN METALIZATION FOR
11157	LSI ARRAYS FOR SPACE STATION ,DESIGN PROCESSING AND TESTING OF
11373	LSI COMPONENTS ,QUALITY MEASURE FOR
11693	LSI DEVICES IN AUTOMOTIVE APPLICATION ,PREDICTING RELIABILITY OF SYSTEMS USING COMPLEX MOS
11195	LSI DEVICES ,CHARGE TRANSPORT AND POLARIZATION EFFECTS IN DIELECTRICS OF MSI AND
11685	LSI FOR AEROSPACE COMPUTERS - PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS ,MOS
11146	LSI MEMORY SYSTEM FOR MILITARY MAINFRAME APPLICATIONS
11678	LSI RADIAC COUNTER CIRCUIT ,NUCLEAR RADIATION EFFECTS ON RCA ECON
11072	LSI - CCCL ,NEW APPROACH TO BIPOLAR
11724	LSI SILICON CHIPS ,MICROSURGERY AS TOOL IN ANALYSIS OF
11264	LSI TAKES NEW DIRECTION WITH IIL ,BIPOLAR
11406	LSI TECHNOLOGY EVALUATION
11064	LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION MOS TRANSISTORS ,HIGH-SPEED LOGIC
11564	LSI ,COMPLEMENTARY DMOS PROCESS FOR
11413	LSI ,CURRENT HOGGING LOGIC - NEW BIPOLAR LOGIC FOR
11657	LSI ,DESIGNERS GUIDE FOR
11141	LSI ,ENGINEERING STUDY OF DEVELOPMENT OF 2-LEVEL ANODIZED ALUMINUM INTERCONNECTS FOR MSI AND
11199	LSI ,STRAPDOWN INERTIAL GUIDANCE USING
11203	MACHINE ,FABRICATION OF VIDEO PROTOTYPE
11472	MACROMODELING OF IC OP-AMPS
11245	MAGNETIC BUBBLE MEMORY
11146	MAINFRAME APPLICATIONS ,LSI MEMORY SYSTEM FOR MILITARY
11603	MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND
11689	MAINTAINABILITY SYMPOSIUM ,PROCEEDINGS 1975 ANNUAL RELIABILITY AND
11594	MANUFACTURE OF HYBRID CIRCUITS ,SELECTION AND CONTROLS OF POLYMERS USED IN
11392	MANUFACTURE ,AUTOMATED METAL ETCH SYSTEM FOR IC
11584	MANUFACTURE ,SEM PROCESS CONTROL OF THIN-FILM AND THICK-FILM MICROCIRCUIT
11601	MANUFACTURER ,FRUSTRATIONS OF LOW COST PACKAGING AS SEEN BY HYBRID CIRCUIT
11353	MANUFACTURING CONTROL HANDBOOK - GUIDE TO FAILURE ANALYSIS AND PROCESS ,MICROCIRCUIT
11299	MANUFACTURING METHODS FOR ION-IMPLANTATION
11418	MANUFACTURING METHODS FOR ION-IMPLANTATIONS
11650	MANUFACTURING METHODS TECHNIQUES AND AUTOMATED CONTROLS FOR CONTINUOUS EPITAXIAL PROCESSING OF SILICON IC'S
11575	MANUFACTURING PROCESS ,MULTILAYER CERAMIC CAPACITOR CHIPS FOR HYBRID CIRCUITS -
11639	MANUFACTURING SCIENCE ,IC RELIABILITY AND
11485	MAPPING OF SEMICONDUCTOR DEVICES ,HIGH RESOLUTION SYSTEM FOR PHOTORESPONSE
11056	MARGINALLY TESTABLE 4K-RAM ,SIMPLIFIED PERIPHERAL CIRCUITS FOR
11391	MASK ALIGNMENT ,AUTOMATIC OUT-OF-CONTACT
11055	MASK DATA ,COMPUTER-AIDED SYNTHESIS OF IC ELECTRICAL DIAGRAM FROM
11386	MASK METROLOGY ,PHOTOLITHOGRAPHY IN IC
11389	MASK PROCESSING TECHNIQUES ,EMULSION
11143	MASS MEMORY ,LOW-POWER CMOS
11571	MATERIAL MICROSTRUCTURE - INFLUENCE OF PROCESSING CONDITIONS ,THICK-FILM
11241	MATERIALS AND PROCESSES PROBLEMS IN THIN-FILM NETWORKS ,DETECTION AND CORRECTION OF

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11642	MATERIALS AS PROTECTIVE COATINGS ON HYBRID MICROCIRCUITS ,APPROACH FOR EVALUATING POLYMER
11238	MATERIALS FOR CONTROLLED COLLAPSE CHIP JOINING ,MODULE
11609	MATERIALS USED IN MICROELECTRONIC DEVICE BONDING ,CHARACTERIZATION OF POLYMERIC
11127	MATERIALS ,EFFECTS OF HIGH ENERGY PULSES ON HYBRID CIRCUIT
11700	MATERIALS ,GOLD CONNECTOR CONTACTS - DEVELOPMENT IN SEARCH FOR ALTERNATE
11460	MATERIALS ,HYBRID TECHNOLOGY LOOSE PARTICLES AND COATING
11544	MATERIALS ,PROBLEMS IN USING SURFACE ANALYSIS TECHNIQUES FOR DEPTH PROFILING OF MICROELECTRONIC
11691	MATURING TECHNOLOGY ,COMPARATIVE RELIABILITY EVALUATION OF CMOS -
11565	MAXIMUM OPERATING VOLTAGE OF CMOS IC'S ,LIMITATIONS ON
11462	MEANS OF ACCELERATED TESTING,PROCESS CONTROL BY
11373	MEASURE FOR LSI COMPONENTS ,QUALITY
11616	MEASUREMENT ACCURACY PRECISION AND REPEATABILITY WITH RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS
11600	MEASUREMENT AND CONTROL OF ATMOSPHERE IN HERMETICALLY SEALED SEMICONDUCTOR PACKAGES
11492	MEASUREMENT OF CHARGE RESIDUAL FOR CCD TRANSFER USING IMPULSE AND FREQUENCY RESPONSES
11487	MEASUREMENT OF LOW DENSITIES OF SURFACE STATES AT SILICON SILICON-DIOXIDE INTERFACE
11635	MEASUREMENT TECHNOLOGY SPREADING RESISTANCE SYMPOSIUM ,SEMICONDUCTOR
11248	MEASUREMENT TECHNOLOGY-400-12,SEMICONDUCTOR
11246	MEASUREMENT TECHNOLOGY-400-4 ,SEMICONDUCTOR
11279	MEASUREMENTS IN ION-IMPLANTED SILICON ,EXCESS NOISE
11542	MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC RAM USING SEM STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM
11372	MEASUREMENTS OF NOISE IN CCD'S
11606	MEASUREMENTS OF SOLDERABILITY OF THICK-FILM CIRCUITS
11322	MEASUREMENTS ON DEPLETION-MODE FET'S AND BULK-TRANSFER CCD'S
11628	MEASUREMENTS ON THIN SILICON-DIOXIDE ,CONTRACT POTENTIAL
11680	MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN SILICON P-N JUNCTIONS ,THERMALLY STIMULATED
11425	MEASUREMENTS ,CHARACTERIZATION OF THERMALLY GROWN SILICON-DIOXIDE SURFACES BY CONTACT ANGLE
11400	MEASUREMENTS ,SOME PITFALLS IN FAST RAMP C-V
11371	MEASURES AUTOMATIC ASSEMBLY OF HYBRID IC'S ,PRODUCTION ENGINEERING
11247	MEASURSMENT TECHNOLOGY-400-8 ,SEMICONDUCTOR
11292	MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF METAL SILICON-DIOXIDE SILICON STRUCTURES UNDER
11589	MECHANICAL THERMAL PULSE BONDING
11742	MECHANISM IN PLASTIC ENCAPSULATED MOS DEVICES ,STUDY OF PARASITIC MOS FORMATION
11452	MECHANISM OF METAL-POLYSILICON DOPED SILICON BUTTINGCONTACTS ,FAILURE
11733	MECHANISM OF NICHROME RESISTOR LINKS IN PROM'S ,FUSING
11447	MECHANISM ,MIGRATORY GOLD RESISTANCE SHORTS - CHEMICAL ASPECTS OF FAILURE
11081	MECHANISMS FOR IC RELIABILITY ,IMPROVED
11385	MECHANISMS IN GOLD METALIZED SEALED JUNCTION ,FAILURE
11435	MECHANISMS IN REWRITABLE N-CHANNEL FAMOS ,DEGRADATION
11714	MECHANISMS IN THICK-FILMS AND THIN-FILMS ,BASIC ADHESION
11719	MECHANISMS OF DEGRADATION IN OPTICALLY-COUPLED ISOLATOR
11734	MECHANISMS OF NICHROME THIN-FILMS ,FUSING
11661	MECHANISMS OF OPTICALLY-COUPLED ISOLATOR ,DEGRADATION CHARACTERISTICS AND
11434	MECHANISMS ,P-CHAINEL REWRITABLE AVALANCHE INJECTION DEVICE OPERATION AND DEGRADATION
11535	MEETING 1975 INTERNATIONAL ELECTRON DEVICES
11318	MEMORIES AND ANALOG SIGNAL PROCESSING ,CCD'S MOVE-IN ON
11415	MEMORIES FOR RADAR
11303	MEMORIES ,ISOLATION METHOD SHRINKS BIPOLAR CELLS FOR FAST DENSE
11626	MEMORIES ,THERMAL OXIDE ISOLATION PROCESS FOR HIGH-DENSITY
11610	MEMORY ARRAYS FOR EFFICIENT HYBRID PACKAGING ,COMPLEX BEAM-LEADED LOGIC AND
11736	MEMORY CELLS ,DUAL DIELECTRIC CHARGE STORAGE NON-VOLATILE
11430	MEMORY CHIPS ,FABRICATION OF BUBBLE
11482	MEMORY CIRCUITS ,PROGRAMMABLE
11511	MEMORY COMES OF AGE ,BIPOLAR
11259	MEMORY DEVICE ,DRAIN-SOURCE PROTECTED MNOS
11293	MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON ,LONG TERM
11267	MEMORY MADE WITH ELECTRON LITHOGRAPHY ,HIGH-SPEED P-CHANNEL RANDOM ACCESS 1024-BIT
11145	MEMORY STATUS AND TRENDS IN US-GOVERNMENT DATA STORAGE APPLICATIONS ,BUBBLE
11146	MEMORY SYSTEM FOR MILITARY MAINFRAME APPLICATIONS ,LSI
11683	MEMORY SYSTEM ,DESIGN AND PERFORMANCE OF CCD
11359	MEMORY TESTING - DIGEST OF TECHNICAL PAPERS ,1973 SYMPOSIUM ON SEMICONDUCTOR
11554	MEMORY WITH METAL NITRIDE MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR
11365	MEMORY WITH MNOS STORAGE ,NON-VOLATILE CCD
11493	MEMORY WITH PHOTOFORMED PLATED CONDUCTORS ,MULTICHIP IC
11469	MEMORY ,8192-BIT BLOCK ADDRESSABLE CCD
11143	MEMORY ,LOW-POWER CMOS MASS
11245	MEMORY ,MAGNETIC BUBBLE
11546	MESHED GATE STRUCTURE ,HIGH-POWER MOS FET WITH VERTICAL DRAIN ELECTRODE AND
11254	METAL ALUMINA SILICON-DIOXIDE SILICON FET ,STUDY OF CHARGE STORAGE BEHAVIOR IN
11402	METAL ALUMINA SILICON-DIOXIDE SILICON ,POLARIZATION AND CHARGE MOTION IN
11392	METAL ETCH SYSTEM FOR IC MANUFACTURE ,AUTOMATED
11554	METAL NITRIDE MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH
11049	METAL OXIDE ELECTRODE CID IMAGER ARRAY ,TRANSPARENT

RAC LIBRARY DOCUMENT TITLE — KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11291	METAL SILICON-DIOXIDE CAPACITORS ,EFFECTS OF DISLOCATIONS ON PROPERTIES OF
11292	METAL SILICON-DIOXIDE SILICON STRUCTURES UNDER MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF
11424	METAL SURFACES ,PLASMA CLEANING OF
11449	METAL SYSTEMS ,EFFECTS OF FAST TEMPERATURE CYCLING ON ALUMINUM AND GOLD
11401	METALIZATION FOR LSI APPLICATIONS ,TUNGSTEN
11387	METALIZATION SYSTEM FOR MICROWAVE AND UHF POWER-TRANSISTORS
11726	METALIZATION ,BERYLLIUM - HIGH-RELIABILITY THIN-FILM
11570	METALIZATION ,CHARACTERIZATION OF THICK-FILM FRITLESS
11385	METALIZED SEALED JUNCTION ,FAILURE MECHANISMS IN GOLD
11623	METALLIC-OXIDE SWITCHES USING THICK-FILM TECHNOLOGY
11148	METALLIZATION CAPACITANCES FOR IC'S AND PACKAGES ,ACCURATE
11573	METALLIZATION FOR THICK-FILM RESISTORS ,IMPROVED SILVER-PALLADIUM TERMINATION
11619	METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK-FILM
11294	METALLIZATION ON SEMICONDUCTORS ,SEM EVALUATION OF
11465	METALLIZATION SYSTEMS VIA ACCELERATED STRESSING ,DETERMINATION OF USEFUL LIFE OF 2-LAYER
11725	METALLIZATION ,EFFECT OF IMPURITIES ON CORROSION OF ALUMINUM
11728	METALLIZATION ,METALLURGICAL ASPECTS OF ALUMINUM WIRE BONDS TO GOLD
11655	METALLIZING FOR CERAMICS ,COMPOSITE FILM
11378	METALLURGICAL ANALYSIS OF STRESS-CORROSION CRACKING OF KOVAR PACKAGE LEADS
11728	METALLURGICAL ASPECTS OF ALUMINUM WIRE BONDS TO GOLD METALLIZATION
11452	METAL-POLYSILICON DOPED SILICON BUTTINGCONTACTS ,FAILURE MECHANISM OF
11429	METHOD-1012 - THERMAL CHARACTERISTICS FOR MIL-STD-883 ,NEW RECOMMENDATION
11380	METHODS AND TECHNIQUES FOR FAILURE ANALYSIS ,APPLICATION OF NEW
11299	METHODS FOR ION-IMPLANTATION ,MANUFACTURING
11418	METHODS FOR ION-IMPLANTATIONS,MANUFACTURING
11301	METHODS FOR PLANNING AND ANALYZING ACCELERATED TESTS
11650	METHODS TECHNIQUES AND AUTOMATED CONTROLS FOR CONTINUOUS EPITAXIAL PROCESSING OF SILICON IC'S ,MANUFACTURING
11297	METHODS TO IC SUSCEPTIBILITY ,APPLICATION OF TIME DOMAIN
11476	METHODS ,EVALUATION OF HIGH-TEMPERATURE ACCELERATED LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING
11231	METHODS ,FAILURE ANALYSIS OF ELECTRONIC PARTS - LABORATORY
11386	METROLOGY ,PHOTOLITHOGRAPHY IN IC MASK
11648	MICROPROBE IN SEMICONDUCTOR FAILURE ANALYSIS ,USE OF ION
11509	MICROPROCESSOR SYSTEMS ,USING BIPOLAR LOGIC TO IMPROVE PERFORMANCE IN CMOS AND
11045	MICROPROCESSOR ,16-BIT
11093	MICROPROCESSORS ,N-CHANNEL MOS TECHNOLOGY YIELDS NEW GENERATION OF
11674	MICRO-POWER DIGITAL AND ANALOG APPLICATIONS ,CMOS PLL - VERSATILE BUILDING BLOCK FOR
11571	MICROSTRUCTURE - INFLUENCE OF PROCESSING CONDITIONS ,THICK-FILM MATERIAL
11729	MICROSUBSTRATES ,INVESTIGATION INTO FAILURES OF ALUMINUM WIRES BONDED TO GOLD METALLIZATION IN
11724	MICROSURGERY AS TOOL IN ANALYSIS OF LSI SILICON CHIPS
11387	MICROWAVE AND UHF POWER-TRANSISTORS,METALIZATION SYSTEM FOR
11545	MICROWAVE HIGH-VOLTAGE BIPOLAR POWER-TRANSISTOR
11097	MICROWAVE IC'S ,BEAM TECHNIQUES FOR FABRICATION OF
11596	MICROWAVE IC'S ,EPOXY TECHNIQUES FOR HYBRID
11382	MICROWAVE POWER-TRANSISTORS,TRENDS IN
11197	MICROWAVE RECEIVERS ,APPLICATION OF IC'S TO
11444	MICROWELDS IN HYBRID MICROCIRCUITS TO CORROSION DEGRADATION ,SUSCEPTIBILITY OF
11446	MIGRATED GOLD RESISTIVE SHORTS IN MICROCIRCUITS
11447	MIGRATORY GOLD RESISTANCE SHORTS - CHEMICAL ASPECTS OF FAILURE MECHANISM
11580	MILITARY APPLICATIONS ,LASER-TRIMMING OF THICK-FILM RESISTORS FOR
11419	MILITARY ELECTRONICS WITH PARTICULAR REFERENCE TO COST AND RELIABILITY-VOL-1,STUDY OF
11695	MILITARY IC STANDARDIZATION ACQUISITION AND TECHNOLOGY
11146	MILITARY MAINFRAME APPLICATIONS ,LSI MEMORY SYSTEM FOR
11429	MIL-STD-883 ,NEW RECOMMENDATION METHOD-1012 - THERMAL CHARACTERISTICS FOR
11441	MINIATURE MOISTURE SENSORS FOR IN-PACKAGE USE BY MICROELECTRONICS INDUSTRY
11130	MINIATURIZATION OF TELEVISION CAMERAS THROUGH HYBRID IC TECHNOLOGY
11085	MINICOMPUTER ON CHIP
11671	MINIMAL POWER DIGITAL DISPLAYS ,LIQUID CRYSTALS AND CMOS OFFER
11649	MINIMIZATION OF PARASITICS IN IC'S BY DIELECTRIC ISOLATION
11496	MIS DEVICES AND IC'S ,INVESTIGATION OF SOS PROCESSES FOR FABRICATION OF RADIATION HARDENED
11270	MIS DEVICES ,LOW-TEMPERATURE IRRADIATION EFFECTS IN SILICON-DIOXIDE INSULATED
11416	MIS IC'S ,INVESTIGATION OF THIN-FILM SILICON PROCESS FOR RADIATION HARDENED
11206	MIS INPUT/OUTPUT SUBSYSTEM DEVELOPMENT ,RADIATION HARDENED
11259	MNOS MEMORY DEVICE ,DRAIN-SOURCE PROTECTED
11059	MNOS RAM USING AVALANCHE-TUNNEL INJECTION ,1024-BIT
11144	MNOS RAM ,1280-BIT
11646	MNOS RELIABILITY AND PROCESS RESEARCH
11652	MNOS STORAGE ARRAYS IN ESFI MOS TECHNOLOGY ,FULLY DECODED
11365	MNOS STORAGE ,NON-VOLATILE CCD MEMORY WITH
11566	MODEL FOR LATERAL THERMAL INSTABILITIES IN POWER-TRANSISTORS,COMPUTER
11543	MODEL YIELD OF IC'S AS FUNCTION OF ACTIVE CIRCUIT AREA ,USE OF POWER TRANSFORMATION TO

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11708 MODELING AND DESIGN ,INTEGRATED DEVICE ANALYSIS
11251 MODELING FOR CIRCUIT DESIGN ,SOS MOS
11567 MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND
11238 MODULE MATERIALS FOR CONTROLLED COLLAPSE CHIP JOINING
11441 MOISTURE SENSORS FOR IN-PACKAGE USE BY MICROELECTRONICS INDUSTRY ,MINIATURE
11554 MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE
11383 MONITORING IN TRANSISTOR PRODUCTION ,PROCESS
11290 MONITORING OF SILICON IC'S ,INVESTIGATION AND DEVELOPMENT OF SHORT-TERM TECHNIQUES FOR RELIABILITY
11515 MONOLITHIC HIGH-PERFORMANCE FET INPUT OP-AMP ,NEW
11275 MONOLITHIC INTEGRATION PROCESS ,CMOS AND COMPLEMENTARY ISOLATED BIPOLAR TRANSISTOR
11190 MONOLITHIC OP-AMP DESIGN ,RECENT ADVANCES IN
11523 MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY PNP TRANSISTORS ,HIGH SLEW RATE
11498 MONOLITHIC OP-AMP USING DOUBLET COMPRESSION TECHNIQUES ,FAST-SETTLING
11258 MONOLITHIC PHOTOSENSOR ARRAYS ,INTERGRATED
11222 MONOLITHIC SEMICONDUCTOR DEVICES BY HIGH-AMPLITUDE CURRENT PULSES ,DEGRADATION OF
11721 MONOLITHIC SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED
11398 MONOLITHIC TECHNOLOGY AND APPLICATIONS ,OXIDE-ISOLATED
11542 MOS 3-TRANSISTOR DYNAMIC RAM USING SEM STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM MEASUREMENTS OF
11271 MOS CAPACITORS ,NON-EQUILIBRIUM PHENOMENA IN ION-IMPLANTED
11486 MOS DEVICES ,NON-IONIC ROOM TEMPERATURE INSTABILITIES IN
11742 MOS DEVICES ,STUDY OF PARASITIC MOS FORMATION MECHANISM IN PLASTIC ENCAPSULATED
11546 MOS FET WITH VERTICAL DRAIN ELECTRODE AND MESHED GATE STRUCTURE ,HIGH-POWER
11742 MOS FORMATION MECHANISM IN PLASTIC ENCAPSULATED MOS DEVICES ,STUDY OF PARASITIC
11274 MOS IC TECHNOLOGY ,VMOS - NEW
11060 MOS IC'S ,FUNDAMENTAL PERFORMANCE LIMITS OF
11319 MOS IC'S ,PROCESSES FOR
11047 MOS IMAGE SENSORS ,ULTRA HIGH-SPEED CLOCK-PULSELESS SCANNER FOR
11375 MOS INPUT AND OUTPUT CIRCUITRY-VOL-I ,HARDENED
11366 MOS LOGIC ,VMOS - HIGH-SPEED TTL COMPATIBLE
11693 MOS LSI DEVICES IN AUTOMOTIVE APPLICATION ,PREDICTING RELIABILITY OF SYSTEMS USING COMPLEX
11685 MOS LSI FOR AEROSPACE COMPUTERS - PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS
11251 MOS MODELING FOR CIRCUIT DESIGN ,SOS
11363 MOS PROCESSING TECHNIQUES ,THEORY AND PRACTICE OF
11379 MOS RAM'S ,DIAGNOSTIC TESTING OF
11663 MOS - RCA PIONEERED TECHNOLOGY CMOS - RCA'S THRUST IN DIGITAL LOGIC
11083 MOS TECHNOLOGY YIELDS NEW GENERATION OF MICROPROCESSORS ,N-CHANNEL
11652 MOS TECHNOLOGY ,FULLY DECODED NMOS STORAGE ARRAYS IN ESFI
11282 MOS TRANSISTORS ,DRAIN VOLTAGE LIMITATIONS OF
11272 MOS TRANSISTORS ,ELECTRICAL CHARACTERISTICS OF BORON-IMPLANTED N-CHANNEL
11064 MOS TRANSISTORS ,HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION
11100 MOS-TRANSISTOR IC ENGINEERING
11402 MOTION IN METAL ALUMINA SILICON-DIOXIDE SILICON ,POLARIZATION AND CHARGE
11329 MOUNTING TECHNOLOGY FOR HYBRIDS ,INVESTIGATION OF DISCRETE COMPONENT CHIP
11318 MOVE-IN ON MEMORIES AND ANALOG SIGNAL PROCESSING ,CCD'S
11193 MSI AND LSI DEVICES ,CHARGE TRANSPORT AND POLARIZATION EFFECTS IN DIELECTRICS OF
11141 MSI AND LSI ,ENGINEERING STUDY OF DEVELOPMENT OF 2-LEVEL ANODIZED ALUMINUM INTERCONNECTS FOR
11493 MULTICHIP IC MEMORY WITH PHOTOFORMED PLATED CONDUCTORS
11575 MULTILAYER CERAMIC CAPACITOR CHIPS FOR HYBRID CIRCUITS - MANUFACTURING PROCESS
11572 MULTILAYER GLASSES NEW CONCEPT ,HIGH-TEMPERATURE VISCOSITY CONTROL IN
11374 MULTILAYER INTERCONNECTION TECHNIQUE FOR IC AND THEIR APPLICATION TO SPACECRAFT ELECTRONIC SYSTEMS
11139 MULTILAYER INTERCONNECTION USING EVAPORATED ALUMINUM CANTILEVERED BEAMS ,FLEXIBLE
11098 MULTILAYERING TECHNIQUE FOR HYBRID MICROCIRCUITS ,THIN-FILM
11457 MULTILEVEL SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT ATTACH FOR HYBRID FABRICATION
11066 MULTIPLEXED VIDEO BANDWIDTH CCD DELAY LINE
11051 MULTIPLEXER ,JFET BIPOLAR 8-CHANNEL ANALOG
11412 MULTIPLEXERS ,FOCUS ON IC ANALOG SWITCHES AND
11293 MULTIVALENT TRAPPING IMPURITIES IN SILICON ,LONG TERM MEMORY IN JUNCTION DEVICES USING
11478 NARROW RESISTIVE LINES TO INCREASE ELECTROMIGRATION RESISTANCE ,COATING
11234 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,1969 PROCEEDINGS OF TECHNICAL PROGRAM -
11687 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,PROCEEDINGS OF TECHNICAL PROGRAM - 1975
11376 NATIONAL SPACEPROGRAM ,HYBRID MICROCIRCUIT TECHNOLOGY IN BRITISH
11426 NATURE OF CONDUCTION AND SWITCHING IN SILICON-DIOXIDE, ON
11549 NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS ,SIMPLE ETCH CONTOUR FOR
11593 NEED FOR STANDARDIZED FORMULATIONS ,CASE FOR BETTER EPOXY PERFORMANCE TESTING AND
11241 NETWORKS ,DETECTION AND CORRECTION OF MATERIALS AND PROCESSES PROBLEMS IN THIN-FILM
11647 NETWORKS ,QUALIFICATION REQUIREMENTS FOR THICK-FILM
11676 NICHROME FUSIBILE-LINK USED IN PROM'S ,RELIABILITY OF
11733 NICHROME RESISTOR LINKS IN PROM'S ,FUSING MECHANISM OF

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11713	NICHROME THIN-FILM STRIPES ,ELECTROMIGRATION FAILURE IN
11734	NICHROME THIN-FILMS ,FUSING MECHANISMS OF
11735	NICHROME-LINK PROM RELIABILITY STUDIES ,PROGRESS REPORT ON
11455	NICHROME-LINK PROMS ,EFFECTS OF PROGRAMMING VARIATIONS ON
11619	NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING
11554	NITRIDE MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL
11569	NITROXIDE BURIED-LAYER THIN-FILM PASSIVATION ,TITANIUM
11063	NMOS EXPERIMENTAL AND THEORETICAL STUDY
11585	NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF
11372	NOISE IN CCD'S ,MEASUREMENTS OF
11266	NOISE IN CHARGE-TRANSFER DEVICES ,THEORY OF
11279	NOISE MEASUREMENTS IN ION-IMPLANTED SILICON ,EXCESS
11271	NON-EQUILIBRIUM PHENOMENA IN ION-IMPLANTED MOS CAPACITORS
11732	NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC CHIP CAPACITORS FOR DELAMINATIONS AND VOIDS
11731	NON-DESTRUCTIVE TEST FOR BEAM-LEAD BOND INTEGRITY ,USE OF ACOUSTIC EMISSION AS
11486	NON-IONIC ROOM TEMPERATURE INSTABILITIES IN MOS DEVICES
11595	NON-LIDDED HYBRID MICROCIRCUITS ,CONFORMAL POLYMER COATING FOR
11736	NON-VOLATILE MEMORY CELLS ,DUAL DIELECTRIC CHARGE STORAGE
11365	NON-VOLATILE CCD MEMORY WITH MNOS STORAGE
11554	NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE
11079	NORMALLY-OFF-TYPE SCHOTTKY BARRIER FET'S ,STATIC RAM WITH
11435	N-CHANNEL FAMOS ,DEGRADATION MECHANISMS IN REWRITABLE
11083	N-CHANNEL MOS TECHNOLOGY YIELDS NEW GENERATION OF MICROPROCESSORS
11272	N-CHANNEL MOS TRANSISTORS ,ELECTRICAL CHARACTERISTICS OF BORON-IMPLANTED
11553	N-CHANNEL SILICON-GATE IC TECHNOLOGY
11300	N-TYPE INVERSION LAYERS IN <100>-SURFACES OF SILICON ,TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN
11321	N-TYPE SOS ,ELASTORESISTANCE OF
11702	NUCLEAR AND ELECTRICAL TECHNIQUES ,ANALYSIS OF SEMICONDUCTOR STRUCTURES BY
11678	NUCLEAR RADIATION EFFECTS ON RCA ECOM LSI RADIAC COUNTER CIRCUIT
11614	OBTAINING OPTIMUM TRIMMING PERFORMANCE FROM LASER SYSTEM ,METHOD OF
11417	OCCURING DURING DEPOSITION OF POLYSILICON FILMS ,DEFORMATION
11135	OCTAVE BANDWIDTH ,UHF HYBRID INTEGRATED 45-WATT 2-STAGE AMPLIFIER WITH
11671	OFFER MINIMAL POWER DIGITAL DISPLAYS ,LIQUID CRYSTALS AND CMOS
11370	OFFERS FLEXIBILITY TO DESIGNER ,ION-IMPLANTATION
11170	ONE-THIRD ,FIRST OXIDE ISOLATED CMOS CIRCUITS CUT CHIP AREA BY
11233	ON-OFF CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND PART RELIABILITY ,DORMANCY AND POWER
11483	OPENING FOR FABRICATING SCHOTTKY-BARRIER DIODE ,CONTACT-HOLE
11464	OPERATING TESTS - CONTROL FOR CONTAMINATED MICROCIRCUIT PROCESSES ,HIGH-TEMPERATURE
11565	OPERATING VOLTAGE OF CMOS IC'S ,LIMITATIONS ON MAXIMUM
11434	OPERATION AND DEGRADATION MECHANISMS ,P-CHANNEL REWRITABLE AVALANCHE INJECTION DEVICE
11473	OPERATION OF FLOATING GATE AMPLIFIER ,DESIGN AND
11190	OP-AMP DESIGN ,RECENT ADVANCES IN MONOLITHIC
11414	OP-AMP SPECS ,BEWARE THOSE FET
1523	OP-AMP USING COMPATIBLE COMPLEMENTARY PNP TRANSISTORS ,HIGH SLEW RATE MONOLITHIC
1498	OP-AMP USING DOUBLET COMPRESSION TECHNIQUES ,FAST-SETTLING MONOLITHIC
11515	OP-AMP ,NEW MONOLITHIC HIGH-PERFORMANCE FET INPUT
11517	OP-AMP ,UNDERSTANDING AND USING UNIQUE CMOS
11472	OP-AMPS ,MACROMODELING OF IC
11522	OP-AMPS ,RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND SETTLING TIME OF
11562	OPTICAL COMMUNICATIONS ,HIGH-POWER LONG-LIVED DOUBLED HETEROSTRUCTURE LED'S FOR
11561	OPTICAL COMMUNICATIONS ,RELIABILITY SEMICONDUCTOR LIGHT SOURCES FOR FIBER
11053	OPTICAL LITHOGRAPHY ,POSITIVE
11661	OPTICALLY-COUPLED ISOLATOR ,DEGRADATION CHARACTERISTICS AND MECHANISMS OF
11719	OPTICALLY-COUPLED ISOLATOR ,MECHANISMS OF DEGRADATION IN
11557	OPTIMIZATION FOR RADIATION HARDNESS ,CMOS
11614	OPTIMUM TRIMMING PERFORMANCE FROM LASER SYSTEM ,METHOD OF OBTAINING
11328	ORGANIC COATINGS IN HYBRIDS ,DESIGN GUIDELINES FOR USE OF ADHESIVES AND
11255	OUT BEST IN CMOS ,SAPPHIRE BRINGS
11375	OUTPUT CIRCUIRTY-VOL-I ,HARDENED MOS INPUT AND
11391	OUT-OF-CONTACT MASK ALIGNMENT ,AUTOMATIC
11479	OVERLAY BY ULTRASONIC PROBE ,ELECTRICAL CONTACT THROUGH SILICON-DIOXIDE
11669	OWN THING - CMOS CUSTOM DESIGN ,DOING YOUR
11439	OXIDATION ,SOS ISLAND EDGE PROFILES FOLLOWING
11567	OXIDE AND DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED
11049	OXIDE ELECTRODE CID IMAGER ARRAY ,TRANSPARENT METAL
11170	OXIDE ISOLATED CMOS CIRCUITS CUT CHIP AREA BY ONE-THIRD ,FIRST
11626	OXIDE ISOLATION PROCESS FOR HIGH-DENSITY MEMORIES ,THERMAL
11653	OXIDE LAYERS BY X-RAY APPEARANCE POTENTIAL SPECTROSCOPY ,INVESTIGATION OF SURFACE
11554	OXIDE SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE MOLYBDENUM
11438	OXIDE TRAPS ,TUNNEL INJECTION INTO GATE
11398	OXIDE-ISOLATED MONOLITHIC TECHNOLOGY AND APPLICATIONS

HAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11636 OXYGEN AND GOLD ON SILICON POWER-DEVICES ,EFFECTS OF
11269 OXYGEN IMPROVES DEVICES ,POLYSILICON LAYER DOPED WITH
11643 OXYGEN ION IMPLEMENTATION ON SILICON SILICON-DIOXIDE INTERFACE PROPERTIES ,EFFECT OF
11692 PACEMAKER SPACE AGE SPIN-OFF TO ACHIEVE RELIABILITY AND LONG LIFE ,MICROCIRCUIT
11603 PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID
11378 PACKAGE LEADS ,METALLURGICAL ANALYSIS OF STRESS-CORROSION CRACKING OF KOVAR
11260 PACKAGES AND ASSEMBLY TECHNIQUES ,MICROCIRCUIT
11458 PACKAGES AND FILM RESISTORS FOR HYBRID MICROCIRCUITS
11124 PACKAGES AND HERMETICALLY SEALED-IN CONTAMINANTS ,IC
11148 PACKAGES ,ACCURATE METALLIZATION CAPACITANCES FOR IC'S AND
11602 PACKAGES ,DESIGN OF FLEXIBILITY OF GLASS WALLED MICROELECTRONICS
11358 PACKAGES ,EVALUATION OF LEAD FINISHES FOR MICROCIRCUIT
11600 PACKAGES ,MEASUREMENT AND CONTROL OF ATMOSPHERE IN HERMETICALLY SEALED SEMICONDUCTOR
11179 PACKAGES ,RELIABILITY EVALUATION OF HERMETIC IC'S IN PLASTIC
11428 PACKAGES ,THERMAL RESISTANCE OF MICROELECTRONIC
11234 PACKAGING AND PRODUCTION CONFERENCE ,1969 PROCEEDINGS OF TECHNICAL PROGRAM - NATIONAL ELECTRONIC
11687 PACKAGING AND PRODUCTION CONFERENCE ,PROCEEDINGS OF TECHNICAL PROGRAM - 1975 NATIONAL ELECTRONIC
11601 PACKAGING AS SEEN BY HYBRID CIRCUIT MANUFACTURER ,FRUSTRATIONS OF LOW COST
11126 PACKAGING SYSTEM AS APPLIED TO ALL APPLICATIONS DIGITAL COMPUTER ,UNIVERSAL
11125 PACKAGING ,BEAM-LEADED INTERCONNECT
11610 PACKAGING ,COMPLEX BEAM-LEADED LOGIC AND MEMORY ARRAYS FOR EFFICIENT HYBRID
11612 PACKAGING ,INTEGRAL LED DISPLAY AND DRIVE CIRCUIT
11707 PACKET RADIO COMMUNICATIONS
11359 PAPERS ,1973 SYMPOSIUM ON SEMICONDUCTOR MEMORY TESTING - DIGEST OF TECHNICAL
11518 PAPERS ,1975 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL
11123 PAPERS ,GOVERNMENT MICROCIRCUIT APPLICATIONS DIGEST OF
11068 PARALLEL INPUT DELAY LINE ARCHITECTURE ,RAZORBACK CCD - HIGH-PERFORMANCE
11605 PARAMETERS FOR BEAM-LEAD BONDING ,CHARACTERIZATION OF THERMOCOMPRESSION BONDING
11587 PARAMETERS ,FINE-LINE SCREEN PRINTING YIELDS AS FUNCTION OF PHYSICAL DESIGN
11722 PARASITIC BIPOLAR ACTION IN IGFET DEVICE ,RELIABILITY IMPLICATIONS OF HOT ELECTRON GENERATION AND
11742 PARASITIC MOS FORMATION MECHANISM IN PLASTIC ENCAPSULATED MOS DEVICES ,STUDY OF
11649 PARASITICS IN IC'S BY DIELECTRIC ISOLATION ,MINIMIZATION OF
11233 PART RELIABILITY ,DORMANCY AND POWER ON-OFF CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND
11460 PARTICLES AND COATING MATERIALS ,HYBRID TECHNOLOGY LOOSE
11419 PARTICULAR REFERENCE TO COST AND RELIABILITY-VOL-I,STUDY OF MILITARY ELECTRONICS WITH
11231 PARTS - LABORATORY METHODS ,FAILURE ANALYSIS OF ELECTRONIC
11442 PARYLENE AS PROTECTIVE SYSTEM FOR MICROCIRCUITY ,TEST OF
11706 PASSIVATION COATINGS ON SILICON DEVICES
11450 PASSIVATION DEFECT STUDY ,INDUCED
11743 PASSIVATION RELIABILITY STUDY ,POLYIMIDE
11569 PASSIVATION ,TITANIUM NITROXIDE BURIED-LAYER THIN-FILM
11685 PAST RELIABILITY EXPERIENCE AND FUTURE PREDICTIONS ,MOS LSI FOR AEROSPACE COMPUTERS
11586 PASTES BY WEIGHT ,CALIBRATION OF THICK-FILM RESISTOR
11536 PATHWAYS AND PITFALLS IN DEVICE LITHOGRAPHY
11633 PC-CARDS ASSEMBLIES ,TESTERS - COMPONENTS IC'S
11614 PERFORMANCE FROM LASER SYSTEM ,METHOD OF OBTAINING OPTIMUM TRIMMING
11509 PERFORMANCE IN C4OS AND MICROPROCESSOR SYSTEMS ,USING BIPOLAR LOGIC TO IMPROVE
11060 PERFORMANCE LIMITS OF MOS IC'S ,FUNDAMENTAL
11683 PERFORMANCE OF CCD MEMORY SYSTEM ,DESIGN AND
11368 PERFORMANCE OF CCD'S ,INFLUENCE OF CLOCK WAVEFORMS ON
11550 PERFORMANCE OF ION-IMPLANTED I2L DEVICES ,FABRICATION AND
11598 PERFORMANCE OF LIQUID EPOXY ENCAPSULANTS IN SEMICONDUCTOR APPLICATIONS
11593 PERFORMANCE TESTING AND NEED FOR STANDARDIZED FORMULATIONS ,CASE FOR BETTER EPOXY
11056 PERIPHERAL CIRCUITS FOR MARGINALLY TESTABLE 4K-RAM ,SIMPLIFIED
11741 PERMEABILITY METHOD FOR EPOXY ENCAPSULATION COMPOUNDS ,DYNAMIC
11137 PHASED ARRAY RADAR APPLICATIONS ,HYBRID INTEGRATED FERRITE PHASE-SHIFTER DRIVER FOR
11137 PHASE-SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS ,HYBRID INTEGRATED FERRITE
11271 PHENOMENA IN ION-IMPLANTED MOS CAPACITORS ,NON-EQUILIBRIUM
11399 PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF SODIUM FROM SILICON-DIOXIDE FILMS BY FORMATION OF
11437 PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY X-RAY
11493 PHOTOFORMED PLATED CONDUCTORS ,MULTICHIP IC MEMORY WITH
11386 PHOTOLITHOGRAPHY IN IC MASK METROLOGY
11388 PHOTOMASKING PROCESS ,TECHNOLOGICAL IMPLICATIONS IN
11298 PHOTORESIST ,SURFACE DESORPTION OF GASES FROM
11485 PHOTORESPONSE MAPPING OF SEMICONDUCTOR DEVICES ,HIGH RESOLUTION SYSTEM FOR
11258 PHOTOSENSOR ARRAYS ,INTEGRATED MONOLITHIC
11454 PHOTOVOLTAGE DETECTION OF DEFECTS IN SILICON WAFERS ,SCANNED SURFACE
11587 PHYSICAL DESIGN PARAMETERS ,FINE-LINE SCREEN PRINTING YIELDS AS FUNCTION OF
11471 PHYSICAL DESIGN PUTS IT ALL TOGETHER ,L5
11656 PHYSICAL PROPERTIES OF THICK SPUTTER-DEPOSITED GLASS FILMS

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11433	PHYSICS PROCEEDINGS ,1975-13TH ANNUAL RELIABILITY
11500	PHYSICS TECHNIQUES ,STUDY OF APPROACHES FOR IMPROVING PRODUCT RELIABILITY THROUGH RELIABILITY
11718	PHYSICS ,1976-14TH ANNUAL PROCEESINGS RELIABILITY
11663	PIONEERED TECHNOLOGY CMOS - RCA'S THRUST IN DIGITAL LOGIC ,MOS - RCA
11536	PITFALLS IN DEVICE LITHOGRAPHY ,PATHWAYS AND
11400	PITFALLS IN FAST RAMP C-V MEASUREMENTS ,SOME
11604	PLAN FOR THICK-FILM PROCESS ,PRACTICAL*QUALITY CONTROL
11549	PLANAR P-N JUNCTIONS ,SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND
11549	PLANE AND PLANAR P-N JUNCTIONS ,SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN
11354	PLANER DIFFUSION SOURCES
11301	PLANNING AND ANALYZING ACCELERATED TESTS ,METHODS FOR
11424	PLASMA CLEANING OF METAL SURFACES
11538	PLASMA ETCHING FOR SEMICONDUCTOR APPLICATIONS ,CHARACTERIZATION OF
11745	PLASTIC AND CERAMIC IC'S WITH THERMAL-SHOCK PRECONDITIONING ,EXTENDED TEMPERATURE CYCLING OF
11742	PLASTIC ENCAPSULATED MOS DEVICES ,STUDY OF PARASITIC MOS FORMATION MECHANISM IN
11179	PLASTIC PACKAGES ,RELIABILITY EVALUATION OF HERMETIC IC'S IN
11493	PLATED CONDUCTORS ,MULTICHIP IC MEMORY WITH PHOTOFORMED
11240	PLATING - EFFECT OF DESIGN SPECIFICATION ,GOLD
11674	PLL - VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS ,CMOS
11512	PLL SYSTEM FOR DATA COMMUNICATIONS ,PRECISION
11362	PMOS COMPUTER DESIGN ,SURVIVABLE
11523	PNP TRANSISTORS ,HIGH SLEW RATE MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY
11402	POLARIZATION AND CHARGE MOTION IN METAL ALUMINA SILICON-DIOXIDE SILICON
11195	POLARIZATION EFFECTS IN DIELECTRICS OF MSI AND LSI DEVICES ,CHARGE TRANSPORT AND
11637	POLYCRYSTALLINE SILICON ISOLATION FOR IC'S
11743	POLYIMIDE PASSIVATION RELIABILITY STUDY
11595	POLYMER COATING FOR NON-LIDDED HYBRID MICROCIRCUITS ,CONFORMAL
11744	POLYMER ENCAPSULANTS ,THERMALLY STIMULATED DISCHARGE EFFECTS IN
11642	POLYMER MATERIALS AS PROTECTIVE COATINGS ON HYBRID MICROCIRCUITS ,APPROACH FOR EVALUATING
11609	POLYMERIC MATERIALS USED IN MICROELECTRONIC DEVICE BONDING ,CHARACTERIZATION OF
11594	POLYMERS USED IN MANUFACTURE OF HYBRID CIRCUITS ,SELECTION AND CONTROLS OF
11427	POLYSILICON ELECTRODES ,IMPROVED DIELECTRIC RELIABILITY OF SILICON-DIOXIDE FILMS WITH
11417	POLYSILICON FILMS ,DEFORMATION OCCURING DURING DEPOSITION OF
11737	POLYSILICON FUSE RELIABILITY
11679	POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED
11679	POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED
11269	POLYSILICON LAYER DOPED WITH OXYGEN IMPROVES DEVICES
11265	POLYSILICON ,ELECTRONIC PROPERTIES OF UNDOPED
11053	POSITIVE OPTICAL LITHOGRAPHY
11641	POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE TRAPPING IN CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF
11592	POSTMORTEM TESTS ,REMOVAL OF HYBRID MICROCIRCUIT BEAM-LEAD DEVICES FOR
11232	POTENTIAL EQUILIBRATION METHOD OF SETTING CHARGE IN CCD'S ,SURFACE
11628	POTENTIAL MEASUREMENTS ON THIN SILICON-DIOXIDE ,CONTRACT
11653	POTENTIAL SPECTROSCOPY ,INVESTIGATION OF SURFACE OXIDE LAYERS BY X-RAY APPEARANCE
11541	POTENTIALS ON IC'S AT HIGH-FREQUENCIES WITH SEM ,QUANTITATIVE DETERMINATION OF SURFACE
11671	POWER DIGITAL DISPLAYS ,LIQUID CRYSTALS AND CMOS OFFER MINIMAL
11547	POWER FET WITH NEW DIFUSSED GATE STRUCTURE ,5000-CHANNEL
11497	POWER HIGH-SPEED CMOS/SOS CIRCUITS ,LOW
11129	POWER HYBRID MICROCIRCUITS FOR HIGH RELIABILITY APPLICATIONS ,DESIGN OF
11233	POWER ON-OFF CYCLING EFFECTS ON ELECTRONIC EQUIPMENT AND PART RELIABILITY ,DORMANCY AND
11543	POWER TRANSFORMATION TO MODEL YIELD OF IC'S AS FUNCTION OF ACTIVE CIRCUIT AREA ,USE OF
11607	POWERFUL CONTROL TOOL FOR THICK-FILM PROCESS ,DESPOSITION WEIGHT -
11103	POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS UNDER CONSTANT AND REVERSED DC
11636	POWER-DEVICES ,EFFECTS OF OXYGEN AND GOLD ON SILICON
11545	POWER-TRANSISTOR ,MICROWAVE HIGH-VOLTAGE BIPOLAR
11566	POWER-TRANSISTORS,COMPUTER MODEL FOR LATERAL THERMAL INSTABILITIES IN
11387	POWER-TRANSISTORS,METALIZATION SYSTEM FOR MICROWAVE AND UHF
11382	POWER-TRANSISTORS,TRENDS IN MICROWAVE
11604	PRACTICAL*QUALITY CONTROL PLAN FOR THICK-FILM PROCESS
11363	PRACTICE OF MOS PROCESSING TECHNIQUES ,THEORY AND
11574	PRATICAL ASPECTS IN DETERMINATION OF THICK-FILM CONDUCTOR RESISTOR SYSTEM USEFUL TO 6-GHZ
11327	PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI GE AND SI-GE ,SOME
11616	PRECISION AND REPEATABILITY WITH RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS ,MEASUREMENT ACCURACY
11512	PRECISION PLL SYSTEM FOR DATA COMMUNICATIONS
11745	PRECONDITIONING ,EXTENDED TEMPERATURE CYCLING OF PLASTIC AND CERAMIC IC'S WITH THERMAL-SHOCK
11693	PREDICTING RELIABILITY OF SYSTEMS USING COMPLEX MOS LSI DEVICES IN AUTOMOTIVE APPLICATION

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11685	PREDICTIONS ,MOS LSI FOR AEROSPACE COMPUTERS - PAST RELIABILITY EXPERIENCE AND FUTURE
11239	PREPARATION OF SUBSTRATES WITH BUMPS FOR FACE-DOWN BONDING OF HYBRID COMPONENTS
11228	PRESEAL VISUAL INSPECTION ,TECHNIQUES OF FINAL
11273	PRESENT AND FUTURE ,IIL -
11194	PRESENTATION ,GENERAL ELECTRIC AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR
11089	PRESENT-DAY STATUS OF ACCELERATED TESTING OF IC'S
11440	PRESSURE - FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK LIDS UNDER EXTERNAL
11302	PRINTED WIRING BOARDS ,TECHNOLOGY AID FABRICATION SUPPORT FOR THICK-FILM MICROELECTRONICS AND
11587	PRINTING YIELDS AS FUNCTION OF PHYSICAL DESIGN PARAMETERS ,FINE-LINE SCREEN
11583	PRINTING ,SCREEN - ESSENTIAL TOOL FOR THICK-FILM
11479	PROBE ,ELECTRICAL CONTACT THROUGH SILICON-DIOXIDE OVERLAY BY ULTRASONIC
11349	PROBLEMS IN APPLICATION OF ALUMINUM ELECTROMIGRATION FAILURE STUDIES ,PRACTICAL
11709	PROBLEMS IN GALLIUM-ARSENIDE ,INVESTIGATION OF TECHNOLOGICAL
11241	PROBLEMS IN THIN-FILM NETWORKS ,DETECTION AND CORRECTION OF MATERIALS AND PROCESSES
11544	PROBLEMS IN USING SURFACE ANALYSIS TECHNIQUES FOR DEPTH PROFILING OF MICROELECTRONIC MATERIALS
11227	PROBLEMS OF CONDUCTION HEAT FLOW IN SOLID-STATE DEVICES ,CTRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF
11689	PROCEEDINGS 1975 ANNUAL RELIABILITY AND MAINTAINABILITY SYMPOSIUM
11234	PROCEEDINGS OF TECHNICAL PROGRAM - NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,1969
11687	PROCEEDINGS OF TECHNICAL PROGRAM - 1975 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE
11433	PROCEEDINGS ,1975-13TH ANNUAL RELIABILITY PHYSICS
11718	PROCEESINGS RELIABILITY PHYSICS ,1976-14TH ANNUAL
11065	PROCESSOR ,SERIAL ANALOG
11395	PROCESSORS ,CCD SIGNAL
11500	PRODUCT RELIABILITY THROUGH RELIABILITY PHYSICS TECHNIQUES ,STUDY OF APPROACHES FOR IMPROVING
11234	PRODUCTION CONFERENCE ,1969 PROCEEDINGS OF TECHNICAL PROGRAM - NATIONAL ELECTRONIC PACKAGING AND
11687	PRODUCTION CONFERENCE ,PROCEEDINGS OF TECHNICAL PROGRAM - 1975 NATIONAL ELECTRONIC PACKAGING AND
11371	PRODUCTION ENGINEERING MEASURES AUTOMATIC ASSEMBLY OF HYBRID IC'S
11597	PRODUCTION OF MICROELECTRONIC COMPONENTS ,USE OF EPOXIES FOR HIGH-VOLUME
11613	PRODUCTION TRIMMING OF FUNCTIONAL HYBRID MICROCIRCUITS ,ACTIVE LASER-TRIMMER FOR
11147	PRODUCTION WITH ELECTRON BEAMS ,IC
11701	PRODUCTION ,FILM CARRIER APPROACHES TO HIGH-VOLUME IC
11383	PRODUCTION ,PROCESS MONITORING IN TRANSISTOR
11688	PROFILE DOUBLE BEAM IC SOCKET ,LOW
11439	PROFILES FOLLOWING OXIDATION ,SOS ISLAND EDGE
11544	PROFILING OF MICROELECTRONIC MATERIALS ,PROBLEMS IN USING SURFACE ANALYSIS TECHNIQUES FOR DEPTH
11160	PROGRAM EFFECTIVENESS ,SCREENING
11475	PROGRAM FOR HARRY DIAMOND LABORATORIES ,BOND IMPROVEMENT
11687	PROGRAM - 1975 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,PROCEEDINGS OF TECHNICAL
11234	PROGRAM - NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE ,1969 PROCEEDINGS OF TECHNICAL
11296	PROGRAM ,COMPUTER GENERATED TROUBLESHOOTING TREES -
11510	PROGRAMMABLE LOGIC ARRAY ,FIELD
11482	PROGRAMMABLE MEMORY CIRCUITS
11455	PROGRAMMING VARIATIONS ON NICHROME-LINK PROMS ,EFFECTS OF
11159	PROGRAMS ,ANALYSIS OF ELECTRONIC COMPONENT SCREENING
11735	PROGRESS REPORT ON NICHROME-LINK PROM RELIABILITY STUDIES
11739	PROM ELEMENTS ,ELECTRICALLY SHORTED SEMICONDUCTOR JUNCTIONS UTILIZED AS
11101	PROM EXPERIENCE
11738	PROM RELIABILITY STUDIES ,FAMOS
11735	PROM RELIABILITY STUDIES ,PROGRESS REPORT ON NICHROME-LINK
11421	PROM RELIABILITY ,SIGNETICS
11182	PROM TECHNOLOGIES ,RELIABILITY ASPECTS OF
11058	PROM WITH 15-NS ACCESS ,1024-BIT ECL
11733	PROM'S ,FUSING MECHANISM OF NICHROME RESISTOR LINKS IN
11740	PROM'S ,RELIABILITY ASSESSMENT OF BIPOLAR
11676	PROM'S ,RELIABILITY OF NICHROME FUSIBILE-LINK USED IN
11455	PROMS ,EFFECTS OF PROGRAMMING VARIATIONS ON NICHROME-LINK
11259	PROTECTED MNOS MEMORY DEVICE ,DRAIN-SOURCE
11642	PROTECTIVE COATINGS ON HYBRID MICROCIRCUITS ,APPROACH FOR EVALUATING POLYMER MATERIALS AS
11442	PROTECTION SYSTEM FOR MICROCIRCUITS, A TEST OF PARYLENE AS A
11203	PROTOTYPE MACHINE ,FABRICATION OF VIDEO
11611	PROTOTYPE ,THICK-FILM HYBRID ELECTRONIC WATCH
11267	P-CHANNEL RANDOM ACCESS 1024-BIT MEMORY MADE WITH ELECTRON LITHOGRAPHY ,HIGH-SPEED
11434	P-CHANNEL REWRITABLE AVALANCHE INJECTION DEVICE OPERATION AND DEGRADATION MECHANISMS
11552	P-CHANNEL SILICON-GATE IC TECHNOLOGY
11549	P-N JUNCTIONS ,SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR
11680	P-N JUNCTIONS ,THERMALLY STIMULATED MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN SILICON

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11589	PULSE BONDING ,MECHANICAL THERMAL
11684	PULSE TESTING OF IC'S ,HIGH-POWER
11295	PULSED-POWER BURNOUT OF IC'S
11127	PULSES ON HYBRID CIRCUIT MATERIALS ,EFFECTS OF HIGH ENERGY
11222	PULSES ,DEGRADATION OF MONOLITHIC SEMICONDUCTOR DEVICES BY HIGH-AMPLITUDE CURRENT
11128	PURPOSE COMPUTER FOR SATELLITE APPLICATIONS ,GENERAL
11471	PUTS IT ALL TOGETHER ,L5 PHYSICAL DESIGN
11647	QUALIFICATION REQUIREMENTS FOR THICK-FILM NETWORKS
11608	QUALITY CONTROL SYSTEM FOR HYBRID MICROELECTRONIC ASSEMBLIES ,SPOT IN-LINE
11480	QUALITY EVALUATING SYSTEM ,AUTOMATIC DIELECTRIC
11373	QUALITY MEASURE FOR LSI COMPONENTS
11054	QUALITY SILICON-DIOXIDE FOR IC'S ,HIGH
11541	QUANTITATIVE DETERMINATION OF SURFACE POTENTIALS ON IC'S AT HIGH-FREQUENCIES WITH SEM
11149	QUESTION ,EPOXY VS EUTECTIC BONDING - STICKY
11162	RAC MICROCIRCUIT WIRE BOND RELIABILITY REPORT ,RE-APPRAISAL OF
11137	RADAR APPLICATIONS ,HYBRID INTEGRATED FERRITE PHASE-SHIFTER DRIVER FOR PHASED ARRAY
11415	RADAR ,MEMORIES FOR
11678	RADIAC COUNTER CIRCUIT ,NUCLEAR RADIATION EFFECTS ON RCA ECOM LSI
11131	RADIATION CHARACTERISTICS OF HARDENED DIGITAL IC FAMILY
11678	RADIATION EFFECTS ON RCA ECOM LSI RADIAC COUNTER CIRCUIT ,NUCLEAR
11369	RADIATION EFFECTS ON SEMICONDUCTOR DEVICES
11223	RADIATION HARD DEVICE SPECS ,FACTS AND FALLACIES OF
11699	RADIATION HARDENED CMOS IC'S ,TOTAL-DOSE
11496	RADIATION HARDENED MIS DEVICES AND IC'S ,INVESTIGATION OF SOS PROCESSES FOR FABRICATION OF
11416	RADIATION HARDENED MIS IC'S ,INVESTIGATION OF THIN-FILM SILICON PROCESS FOR
11206	RADIATION HARDENED MIS INPUT/OUTPUT SUBSYSTEM DEVELOPMENT
11557	RADIATION HARDNESS ,CMOS OPTIMIZATION FOR
11679	RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF
11134	RADIATION RESISTANCE OF CMOS CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE GATE DIELECTRICS
11394	RADIATION RESISTANT CMOS SOS CIRCUITRY
11520	RADIATION SCREENING OF MICROCIRCUITS FOR LONG LIFE APPLICATIONS ,ELECTROMAGNETIC
11133	RADIATION TOLERANT GATED VIDEO AMPLIFIER
11654	RADIATION ,SURFACE CLEANING BY ULTRAVIOLET
11467	RADIATION-EFFECTS ON SEMICONDUCTOR DEVICES ,X-RAY
11707	RADIO COMMUNICATIONS ,PACKET
11732	RADIOGRAPHIC INSPECTION OF CERAMIC CHIP CAPACITORS FOR DELAMINATIONS AND VOIDS ,NON-DESTRUCTIVE
11514	RAM TESTING ,BIPOLAR ECL AND TTL
11059	RAM USING AVALANCHE-TUNNEL INJECTION ,1024-BIT MNOS
11542	RAM USING SEM STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC
11079	RAM WITH NORMALLY-OFF-TYPE SCHOTTKY BARRIER FET'S ,STATIC
11144	RAM ,1280-BIT MNOS
11057	RAM ,4096-BIT HIGH-SPEED ECL COMPATIBLE
11432	RAM ,CCD LINE ADDRESSABLE
11516	RAMP A/D-CONVERTERS ,APPLICATIONS OF DUAL
11400	RAMP C-V MEASUREMENTS ,SOME PITFALLS IN FAST
11379	RAM'S ,DIAGNOSTIC TESTING OF MOS
11084	RAM'S ,SEMICONDUCTOR
11267	RANDOM ACCESS 1024-BIT MEMORY MADE WITH ELECTRON LITHOGRAPHY ,HIGH-SPEED P-CHANNEL
11523	RATE MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY PNP TRANSISTORS ,HIGH SLEW
11068	RAZORBACK CCD - HIGH-PERFORMANCE PARALLEL INPUT DELAY LINE ARCHITECTURE
11662	RCA CMOS TECHNOLOGY
11678	RCA ECOM LSI RADIAC COUNTER CIRCUIT ,NUCLEAR RADIATION EFFECTS ON
11663	RCA PIONEERED TECHNOLOGY CMOS - RCA'S THRUST IN DIGITAL LOGIC ,MOS -
11663	RCA'S THRUST IN DIGITAL LOGIC ,MOS - RCA PIONEERED TECHNOLOGY CMOS -
11075	RECEIVERS USING I2L TECHNIQUES ,VERTICAL SYNCHRONIZING CIRCUIT FOR TV
11197	RECEIVERS ,APPLICATION OF IC'S TO MICROWAVE
11537	RECENT ADVANCES IN HIGH-FREQUENCY FET'S
11190	RECENT ADVANCES IN MONOLITHIC OP-AMP DESIGN
11390	RECENT SOS TECHNOLOGY ADVANCES AND APPLICATIONS
11429	RECOMMENDATION METHOD-1012 - THERMAL CHARACTERISTICS FOR MIL-STD-883 ,NEW
11440	RECTANGULAR FLAT-PACK LIDS UNDER EXTERNAL PRESSURE - FORMULAS FOR SCREENING AND DESIGN
11069	RECURSIVE FILTERS ,DUAL DIFFERENTIAL ANALOG CCD FOR TIME SHARED
11470	REDUCED GAIN OF ION-IMPLANTED TRANSISTORS
11419	REFERENCE TO COST AND RELIABILITY-VOL-I,STUDY OF MILITARY ELECTRONICS WITH PARTICULAR
11491	REFILL TECHNIQUES AND DECAL AIR ISOLATION ,ISOLATION TECHNIQUES FOR FABRICATING IC'S - DIELECTRIC
11622	REFLECTION FOR CHARACTERIZATION OF ELECTRONIC FILMS ,ATTENUATED TOTAL INFRARED INTERNAL
11320	REGIONS ON ELECTRICAL CONDUCTIVITY OF EXTRINSIC SEMICONDUCTOR FILMS ,EFFECT OF SURFACE
11629	REGIONS ,DIELECTRIC ISOLATION OF SILICON
11381	RELATED ELECTRON BEAM TECHNIQUES IN IC TECHNOLOGY ,SEM AND
11522	RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND SETTLING TIME OF OP-AMPS
11618	RELATIONSHIPS IN SOLAR INTERCONNECTIONS ,TIME-DEPENDENT
11616	RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS ,MEASUREMENT ACCURACY PRECISION AND REPEATABILITY WITH
11419	RELIABILITY-VOL-I,STUDY OF MILITARY ELECTRONICS WITH PARTICULAR REFERENCE TO COST AND

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11548	RELIABLE HIGH-VOLTAGE TRANSISTORS ,HIGHLY
11243	RELIABILITY CRITERIA- USER VIEW-POINT ,ALUMINA SUBSTRATES
11327	REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI GE AND SI-GE ,SOME PRATICAL
11090	REMELTING OF CRYSTALS IN GLASS ,FORMATION OF BUBBLES DURING DEVITRIFICATION AND
11592	REMOVAL OF HYBRID MICROCIRCUIT BEAM-LEAD DEVICES FOR POSTMORTEM TESTS
11399	REMOVAL OF SODIUM FROM SILICON-DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE
11459	REPAIRS TO COMPLEX HYBRID CIRCUITS - THEIR EFFECT ON RELIABILITY
11616	REPEATABILITY WITH RELEVANCE TO ELECTRICAL TESTING OF MICROCIRCUITS ,MEASUREMENT ACCURACY PRECISION AND
11735	REPORT ON NICHROME-LINK PROM RELIABILITY STUDIES ,PROGRESS
11162	REPORT ,RE-APPRAISAL OF RAC MICROCIRCUIT WIRE BOND R LIABILITY
11067	REPROGRAMMABLE FILTER BANK USING CCD DISCRETE ANALOG SIGNAL PROCESSING
11554	REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE MOLYBDENUM OXIDE SILICON STRUCTURE ,ELECTRICALLY
11281	REPROGRAMMABLE ROM DEVICE ,ATMOS - ELECTRICALLY
11647	REQUIREMENTS FOR THICK-FILM NETWORKS ,QUALIFICATION
11162	RE-APPRAISAL OF RAC MICROCIRCUIT WIRE BOND RELIABILITY REPORT
11646	RESEARCH ,MOS RELIABILITY AND PROCESS
11492	RESIDUAL FOR CCD TRANSFER USING IMPULSE AND FREQUENCY RESPONSES ,MEASUREMENT OF CHARGE
11591	RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN FILM GOLD ,CHANGES IN STRENGTH AND
11134	RESISTANCE OF CMOS CIRCUITS MADE WITH ALUMINA SILICON-DIOXIDE GATE DIELECTRICS ,RADIATION
11428	RESISTANCE OF MICROELECTRONIC PACKAGES ,THERMAL
11585	RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING
11447	RESISTANCE SHORTS - CHEMICAL ASPECTS OF FAILURE MECHANISM ,MIGRATORY GOLD
11635	RESISTANCE SYMPOSIUM ,SEMICONDUCTOR MEASUREMENT TECHNOLOGY SPREADING
11478	RESISTANCE ,COATING NARROW RESISTIVE LINES TO INCREASE ELECTROMIGRATION
11394	RESISTANT CMOS SOS CIRCUITRY ,RADIATION
11478	RESISTIVE LINES TO INCREASE ELECTROMIGRATION RESISTANCE ,COATING NARROW
11446	RESISTIVE SHORTS IN MICROCIRCUITS ,MIGRATED GOLD
11733	RESISTOR LINKS IN PROMS ,FUSING MECHANISM OF NICHROME
11586	RESISTOR PASTES BY WEIGHT ,CALIBRATION OF THICK-FILM
11574	RESISTOR SYSTEM USEFUL TO 6-GHZ ,PRATICAL ASPECTS IN DETERMINATION OF THICK-FILM CONDUCTOR
11458	RESISTORS FOR HYBRID MICROCIRCUITS ,PACKAGES AND FILM
11580	RESISTORS FOR MILITARY APPLICATIONS ,LASER-TRIMMING OF THICK-FILM
11585	RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM
11483	RESISTORS WITH IMPROVED VOLTAGE STABILITY ,THICK-FILM
11573	RESISTORS ,IMPROVED SILVER-PALLADIUM TERMINATION METALLIZATION FOR THICK-FILM
11579	RESISTORS ,ON LASER-TRIMMING OF THICK-FILM AND THIN-FILM
11576	RESISTORS ,ULTRA LOW-OHM CHIP
11485	RESOLUTION SYSTEM FOR PHOTORESPONSE MAPPING OF SEMICONDUCTOR DEVICES ,HIGH
11522	RESPONSE AND SETTLING TIME OF OP-AMPS ,RELATIONSHIP BETWEEN FREQUENCY
11492	RESPONSES ,MEASUREMENT OF CHARGE RESIDUAL FOR CCD TRANSFER USING IMPULSE AND FREQUENCY
11585	RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT
11103	REVERSED DC POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS UNDER CONSTANT AND
11640	REVIEW OF LIMITATIONS OF ALUMINUM THIN-FILMS ON SEMICONDUCTOR DEVICES
11634	REVIEW - BONDING ,EQUIPMENT
11668	REVOLUTION THROUGH CMOS TECHNOLOGY ,TIMEKEEPING
11681	REWORK OF LINEAR IC'S
11434	REWRITABLE AVALANCHE INJECTION DEVICE OPERATION AND DEGRADATION MECHANISMS ,P-CHANNEL
11435	REWRITABLE N-CHANNEL FAMOS ,DEGRADATION MECHANISMS IN
11677	RF HYBRID MICROCIRCUIT SOLDERING TECHNIQUES
11690	RF IC'S ,DEVELOPMENT OF BEAM-LEAD
11407	RF KEYED CROSSED FIELD AMPLIFIER ,DEVELOPMENT OF HIGH RELIABILITY
11697	RIBBON WIRE VERSUS ROUND WIRE RELIABILITY FOR HYBRID MICROCIRCUITS
11281	ROM DEVICE ,ATMOS - ELECTRICALLY REPROGRAMMABLE
11486	ROOM TEMPERATURE INSTABILITIES IN MOS DEVICES ,NON-IONIC
11697	ROUND WIRE RELIABILITY FOR HYBRID MICROCIRCUITS ,RIBBON WIRE VERSUS
11300	-100-SURFACES OF SILICON ,TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN N-TYPE INVERSION LAYERS IN
11256	SAPPHIRE BRINGS OUT BEST IN CMOS
11128	SATELLITE APPLICATIONS ,GENERAL PURPOSE COMPUTER FOR
11423	SATELLITIES ,USE OF IC'S IN FUTURE
11454	SCANNED SURFACE PHOTOVOLTAGE DETECTION OF DEFECTS IN SILICON WAFERS
11047	SCANNER FOR MOS IMAGE SENSORS ,ULTRA HIGH-SPEED CLOCK-PULSELESS
11540	SCANNING OF ACTIVE SEMICONDUCTOR DEVICES ,LASER
11682	SCHEDULE FOR BEAM-LEAD DEVICES ,ANALYSIS AND DEVELOPMENT OF THERMO-COMPRESSIONBOND
11079	SCHOTTKY BARRIER FET'S ,STATIC RAM WITH NORMALLY-OFF-TYPE
11468	SCHOTTKY IIL
11073	SCHOTTKY TRANSISTOR LOGIC
11104	SCHOTTKY TTL ,LOW-POWER
11483	SCHOTTKY-BARRIER DIODE ,CONTACT-HOLE OPENING FOR FABRICATING

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11639	SCIENCE ,IC RELIABILITY AND MANUFACTURING
11620	SCREEN FOR HIGH-RELIABILITY HYBRID CIRCUITS ,ELECTRICAL
11587	SCREEN PRINTING YIELDS AS FUNCTION OF PHYSICAL DESIGN PARAMETERS ,FINE-LINE
11583	SCREEN - ESSENTIAL TOOL FOR THICK-FILM PRINTING
11440	SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK LIDS UNDER EXTERNAL PRESSURE - FORMULAS FOR
11476	SCREENING METHODS ,EVALUATION OF HIGH-TEMPERATURE ACCELERATED LIFE TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT
11520	SCREENING OF MICROCIRCUITS FOR LONG LIFE APPLICATIONS ,ELECTROMAGNETIC RADIATION
11160	SCREENING PROGRAM EFFECTIVENESS
11159	SCREENING PROGRAMS ,ANALYSIS OF ELECTRONIC COMPONENT
11632	SCREENPRINTING THICK-FILM ,TECHNOLOGY ASSESSMENT -
11224	SEAL TESTING ,INVESTIGATION OF MICROCIRCUIT
11208	SEALED JUNCTION DEVICES ,RELIABILITY STUDY OF BEAM-LEAD
11621	SEALED JUNCTION DEVICES ,RELIABILITY OF BEAM-LEAD
11385	SEALED JUNCTION ,FAILURE MECHANISMS IN GOLD METALIZED
11600	SEALED SEMICONDUCTOR PACKAGES ,MEASUREMENT AND CONTROL OF ATMOSPHERE IN HERMETICALLY
11124	SEALED-IN CONTAMINANTS ,IC PACKAGES AND HERMETICALLY
11443	SEALING GLASSES WITH EXTENDED THERMAL CYCLING ,DEGRADATION OF BONDING WIRES AND
11603	SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH YIELDS IN HYBRID PACKAGE HERMETIC
11700	SEARCH FOR ALTERNATE MATERIALS ,GOLD CONNECTOR CONTACTS - DEVELOPMENT IN
11601	SEEN BY HYBRID CIRCUIT MANUFACTURER ,FRUSTRATIONS OF LOW COST PACKAGING AS
11594	SELECTION AND CONTROLS OF POLYMERS USED IN MANUFACTURE OF HYBRID CIRCUITS
11064	SELF-ALIGNED ENHANCEMENT DEPLETION MOS TRANSISTORS ,HIGH-SPEED LOGIC LSI USING DIFFUSION
11436	SELF-QUENCHING TECHNIQUE ,STUDY OF DIELECTRIC BREAKDOWN OF THERMALLY GROWN SILICON-DIOXIDE BY
11381	SEM AND RELATED ELECTRON BEAM TECHNIQUES IN IC TECHNOLOGY
11294	SEM EVALUATION OF METALLIZATION ON SEMICONDUCTORS
11584	SEM PROCESS CONTROL OF THIN-FILM AND THICK-FILM MICROCIRCUIT MANUFACTURE
11542	SEM STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC RAM USING
11541	SEM ,QUANTITATIVE DETERMINATION OF SURFACE POTENTIALS ON IC'S AT HIGH-FREQUENCIES WITH
11364	SEMICONDUCTING PROPERTIES OF THIN-FILMS OF SOS AND SPINEL ,COMPARSION OF
11250	SEMICONDUCTOR-DEVICE RELIABILITY ,ELEMENTS OF
11061	SENSE-AMPLIFIER ,HIGH-SENSITIVITY CHARGE-TRANSFER
11585	SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE
11441	SENSORS FOR IN-PACKAGE USE BY MICROELECTRONICS INDUSTRY ,MINIATURE MOISTURE
11047	SENSORS ,ULTRA HIGH-SPEED CLOCK-PULSELESS SCANNER FOR MOS IMAGE
11065	SERIAL ANALOG PROCESSOR
11456	SESSIONS ON HYBRID TECHNOLOGY INTRODUCTION ,TUTORIAL
11232	SETTING CHARGE IN CCD'S ,SURFACE POTENTIAL EQUILIBRATION METHOD OF
11522	SETTLING TIME OF OP-AMPS ,RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND
11069	SHARED RECURSIVE FILTERS ,DUAL DIFFERENTIAL ANALOG CCD FOR TIME
11739	SHORTED SEMICONDUCTOR JUNCTIONS UTILIZED AS PROM ELEMENTS ,ELECTRICALLY
11290	SHORT-TERM TECHNIQUES FOR RELIABILITY MONITORING OF SILICON IC'S ,INVESTIGATION AND DEVELOPMENT OF
11560	SHORTS IN BIPOLAR DEVICES ,EMITTER COLLECTOR
11446	SHORTS IN MICROCIRCUITS ,MIGRATED GOLD RESISTIVE
11447	SHORTS - CHEMICAL ASPECTS OF FAILURE MECHANISM ,MIGRATORY GOLD RESISTANCE
11303	SHRINKS BIPOLAR CELLS FOR FAST DENSE MEMORIES ,ISOLATION METHOD
11327	SI GE AND SI-GE ,SOME PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF
11490	SIGNAL PROCESSING ,CCD ANALOG
11703	SIGNAL PROCESSING ,CCD'S IN ANALOG
11318	SIGNAL PROCESSING ,CCD'S MOVE-IN ON MEMORIES AND ANALOG
11067	SIGNAL PROCESSING ,REPROGRAMMABLE FILTER BANK USING CCD DISCRETE ANALOG
11395	SIGNAL PROCESSORS ,CCD
11644	SIGNATURES FOR ANALYSIS OF DIGITAL CIRCUITS ,INFRARED
11421	SIGNETICS PROM RELIABILITY
11277	SILICA SUBSTRATES ,VACUUM DEPOSITED SILICON DEVICES ON FUSED
11452	SILICON BUTTINGCONTACTS ,FAILURE MECHANISM OF METAL-POLYSILICON DOPED
11724	SILICON CHIPS ,MICROSURGERY AS TOOL IN ANALYSIS OF LSI
11277	SILICON DEVICES ON FUSED SILICA SUBSTRATES ,VACUUM DEPOSITED
11706	SILICON DEVICES ,PASSIVATION COATINGS ON
11399	SILICON-DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF SODIUM FROM
11254	SILICON FET ,STUDY OF CHARGE STORAGE BEHAVIOR IN METAL ALUMINA SILICON-DIOXIDE
11290	SILICON IC'S ,INVESTIGATION AND DEVELOPMENT OF SHORT-TERM TECHNIQUES FOR RELIABILITY MONITORING OF
11650	SILICON IC'S ,MANUFACTURING METHODS TECHNIQUES AND AUTOMATED CONTROLS FOR CONTINUOUS EPITAXIAL PROCESSING OF
11721	SILICON IC'S ,STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED MONOLITHIC
11076	SILICON IMAGING DEVICE ,512X320-ELEMENT
11437	SILICON INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE
11637	SILICON ISOLATION FOR IC'S ,POLYCRYSTALLINE

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11636 SILICON POWER-DEVICES ,EFFECTS OF OXYGEN AND COLD ON
11416 SILICON PROCESS FOR RADIATION HARDENED MIS IC'S ,INVESTIGATION OF THIN-FILM
11680 SILICON P-N JUNCTIONS ,THERMALLY STIMULATED MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN
11629 SILICON REGIONS ,DIELECTRIC ISOLATION OF
11643 SILICON SILICON-DIOXIDE INTERFACE PROPERTIES ,EFFECT OF OXYGEN ION IMPLEMENTATION ON
11487 AT SILICON SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF LOW DENSITIES OF SURFACE STATES AT
11675 SILICON SLICE ANALYSER USING HELIUM-NEON LASER
11554 SILICON STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE MOLYBDENUM OXIDE
11292 SILICON STRUCTURES UNDER MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF METAL SILICON-DIOXIDE
11454 SILICON WAFERS ,SCANNED SURFACE PHOTOVOLTAGE DETECTION OF DEFECTS IN
11142 SILICON ,DEVICE IMPLICATIONS OF ION-IMPLANTATION DAMAGE IN
11641 SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE TRAPPING IN CVD-ALUMINA FILMS ON
11279 SILICON ,EXCESS NOISE MEASUREMENTS IN ION-IMPLANTED
11293 SILICON ,LONG TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN
11402 SILICON ,POLARIZATION AND CHARGE MOTION IN METAL ALUMINA SILICON-DIOXIDE
11300 SILICON ,TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN N-TYPE INVERSION LAYERS IN -TWO-SURFACES OF
11436 SILICON-DIOXIDE BY SELF-QUENCHING TECHNIQUE ,STUDY OF DIELECTRIC BREAKDOWN OF THERMALLY GROWN
11291 SILICON-DIOXIDE CAPACITORS ,EFFECTS OF DISLOCATIONS ON PROPERTIES OF METAL
11427 SILICON-DIOXIDE FILMS WITH POLYSILICON ELECTRODES ,IMPROVED DIELECTRIC RELIABILITY OF
11054 SILICON-DIOXIDE FOR IC'S ,HIGH QUALITY
11134 SILICON-DIOXIDE GATE DIELECTRICS ,RADIATION RESISTANCE OF CMOS CIRCUITS MADE WITH ALUMINA -
11270 SILICON-DIOXIDE INSULATED MIS DEVICES ,LOW-TEMPERATURE IRRADIATION EFFECTS IN
11643 SILICON-DIOXIDE INTERFACE PROPERTIES ,EFFECT OF OXYGEN ION IMPLEMENTATION ON SILICON
11479 SILICON-DIOXIDE OVERLAY BY ULTRASONIC PROBE ,ELECTRICAL CONTACT THROUGH
11254 SILICON-DIOXIDE SILICON FET ,STUDY OF CHARGE STORAGE BEHAVIOR IN METAL ALUMINA
11437 SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT
11292 SILICON-DIOXIDE SILICON STRUCTURES UNDER MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF METAL
11402 SILICON-DIOXIDE SILICON ,POLARIZATION AND CHARGE MOTION IN METAL ALUMINA
11425 SILICON-DIOXIDE SURFACES BY CONTACT ANGLE MEASUREMENTS ,CHARACTERIZATION OF THERMALLY GROWN
11628 SILICON-DIOXIDE ,CONTRACT POTENTIAL MEASUREMENTS ON THIN
11553 SILICON-GATE IC TECHNOLOGY ,N-CHANNEL
11552 SILICON-GATE IC TECHNOLOGY ,P-CHANNEL
11651 SILICON-NITRIDE FILM THICKNESS ON BIPOLAR TRANSISTOR CHARACTERISTICS ,DEPENDENCE OF
11348 SILICON-ON-SUBSTRATE IC TECHNOLOGY
11487 SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF LOW DENSITIES OF SURFACE STATES AT SILICON
11453 SILVER CONDUCTORS ,WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN ALUMINUM-COPPER AL-CU-SI AND
11573 SILVER-PALLADIUM TERMINATION METALLIZATION FOR THICK-FILM RESISTORS ,IMPROVED
11549 SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS
11056 SIMPLIFIED PERIPHERAL CIRCUITS FOR MARGINALLY TESTABLE 4K-RAM
11666 SIMPLIFIES EQUIPMENT DESIGN ,CMOS
11284 SINKS ,THERMAL PROPERTIES OF ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT
11327 SI-GE ,SOME PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI GE AND
11437 SITES AT SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT
11523 SLEW RATE MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY PNP TRANSISTORS ,HIGH
11675 SLICE ANALYSER USING HELIUM-NEON LASER ,SILICON
11578 SMALL BUMP FLIP-CHIPS ,SEMICONDUCTOR CHIP ATTACHMENT WITH
11688 SOCKET ,LOW PROFILE DOUBLE BEAM IC
11399 SODIUM FROM SILICON-DIOXIDE FILMS BY FORMATION OF PHOSPHOSILICATE GLASS ,COMPLETE REMOVAL OF
11437 SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY X-RAY PHOTOELECTRON SPECTROSCOPY
11618 SOLAR INTERCONNECTIONS ,TIME-DEPENDENT RELATIONSHIPS IN
11577 SOLDER BUMP FLIP-CHIP FABRICATION USING CIRCUIT LAYOUT
11109 SOLDER GLASS TECHNOLOGY ,ADVANCES IN
11619 SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF
11606 SOLDERABILITY OF THICK-FILM CIRCUITS ,MEASUREMENTS OF
11677 SOLDERING TECHNIQUES ,RF HYBRID MICROCIRCUIT
11191 SOLID ENCAPSULATED MICROCIRCUITS FOR LONG LIFE APPLICATIONS ,STUDY OF
11262 SOLID-STATE TECHNOLOGY ,HIGHLIGHTS -
11518 SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS ,1975 IEEE INTERNATIONAL
11704 SOLID-STATE DEVICES ,CONTROL OF ELECTROSTATIC DAMAGE TO

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11694	TESTING OF IC'S ,EVALUATION
11684	TESTING OF IC'S ,HIGH-POWER PULSE
11089	TESTING OF IC'S ,PRESENT-DAY STATUS OF ACCELERATED
11627	TESTING OF INCOMING DIGITAL DEVICES ,AUTOMATIC
11157	TESTING OF LSI ARRAYS FOR SPACE STATION ,DESIGN PROCESSING AND
11676	TESTING OF MICROCIRCUITS ,MEASUREMENT ACCURACY PRECISION AND REPEATABILITY WITH RELEVANCE TO ELECTRICAL
11379	TESTING OF MOS RAM'S ,DIAGNOSTIC
11359	TESTING - DIGEST OF TECHNICAL PAPERS ,1973 SYMPOSIUM ON SEMICONDUCTOR MEMORY
11088	TESTING TENSILE STRENGTH OF THERMOCOMPRESSION BONDS ,TECHNIQUE FOR
11514	TESTING ,BIPOLAR ECL AND TTL RAM
11224	TESTING .INVESTIGATION OF MICROCIRCUIT SEAL
11393	TESTING ,WAFER
11464	TESTS - CONTROL FOR CONTAMINATED MICROCIRCUIT PROCESSES ,HIGH-TEMPERATURE OPERATING
11301	TESTS ,METHODS FOR PLANNING AND ANALYZING ACCELERATED
11592	TESTS ,REMOVAL OF HYBRID MICROCIRCUIT BEAM-LEAD DEVICES FOR POSTMORTEM
11374	THEIR APPLICATION TO SPACECRAFT ELECTRONIC SYSTEMS ,MULTILAYER INTERCONNECTION TECHNIQUE FOR IC AND
11459	THEIR EFFECT ON RELIABILITY ,REPAIRS TO COMPLEX HYBRID CIRCUITS -
11063	THEORETICAL STUDY ,NMOS EXPERIMENTAL AND
11429	THERMAL CHARACTERISTICS FOR MIL-STD-883 ,NEW RECOMMENDATION METHOD-1012 -
11443	THERMAL CYCLING ,DEGRADATION OF BONDING WIRES AND SEALING GLASSES WITH EXTENDED
11253	THERMAL DEMANDS OF ELECTRONIC DESIGN
11566	THERMAL INSTABILITIES IN POWER-TRANSISTORS,COMPUTER MODEL FOR LATERAL
11626	THERMAL OXIDE ISOLATION PROCESS FOR HIGH-DENSITY MEMORIES
11284	THERMAL PROPERTIES OF ANNULAR AND ARRAY GEOMETRY SEMICONDUCTOR DEVICES ON COMPOSITE HEAT SINKS
11589	THERMAL PULSE BONDING ,MECHANICAL
11428	THERMAL RESISTANCE OF MICROELECTRONIC PACKAGES
11436	THERMALLY GROWN SILICON-DIOXIDE BY SELF-QUENCHING TECHNIQUE ,STUDY OF DIELECTRIC BREAKDOWN OF
11425	THERMALLY GROWN SILICON-DIOXIDE SURFACES BY CONTACT ANGLE MEASUREMENTS ,CHARACTERIZATION OF
11744	THERMALLY STIMULATED DISCHARGE EFFECTS IN POLYMER ENCAPSULANTS
11680	THERMALLY STIMULATED MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN SILICON P-N JUNCTIONS
11745	THERMAL-SHOCK PRECONDITIONING ,EXTENDED TEMPERATURE CYCLING OF PLASTIC AND CERAMIC IC'S WITH
11198	THERMIONIC CIRCUITS ,INTEGRATED
11711	THERMOCOMPRESSION BONDABILITY OF GOLD ,EFFECT OF SURFACE CONTAMINATION ON
11605	THERMOCOMPRESSION BONDING PARAMETERS FOR BEAM-LEAD BONDING ,CHARACTERIZATION OF
11625	THERMOCOMPRESSION BONDING ,HIGH-TEMPERATURE DEFORMATION PROPERTIES OF GOLD
11712	THERMOCOMPRESSION BONDING ,ON CHEMICAL CLEANING FOR
11088	THERMOCOMPRESSION BONDS ,TECHNIQUE FOR TESTING TENSILE STRENGTH OF
11581	THERMOPLASTIC DIELECTRIC PROCESS ,SEMICONDUCTOR
11682	THERMO-COMPRESSIONBOND SCHEDULE FOR BEAM-LEAD DEVICES ,ANALYSIS AND DEVELOPMENT OF
11656	THICK SPUTTER-DEPOSITED GLASS FILMS ,PHYSICAL PROPERTIES OF
11651	THICKNESS ON BIPOLAR TRANSISTOR CHARACTERISTICS ,DEPENDENCE OF SILICON-NITRIDE FILM
11591	THICK-FILM AND THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO
11579	THICK-FILM AND THIN-FILM RESISTORS ,ON LASER-TRIMMING OF
11606	THICK-FILM CIRCUITS ,MEASUREMENTS OF SOLDERABILITY OF
11574	THICK-FILM CONDUCTOR RESISTOR SYSTEM USEFUL TO 6-GHZ ,PRACTICAL ASPECTS IN DETERMINATION OF
11588	THICK-FILM CONDUCTORS ,RELIABILITY CONSIDERATION FOR ULTRASONIC WIRE BONDING ON
11570	THICK-FILM FRITLESS METALIZATION ,CHARACTERIZATION OF
11611	THICK-FILM HYBRID ELECTRONIC WATCH PROTOTYPE
11237	THICK-FILM HYBRID IC'S
11571	THICK-FILM MATERIAL MICROSTRUCTURE - INFLUENCE OF PROCESSING CONDITIONS
11619	THICK-FILM METALLIZATION ON CERAMIC SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO
11584	THICK-FILM MICROCIRCUIT MANUFACTURE ,SEM PROCESS CONTROL OF THIN-FILM AND
11302	THICK-FILM MICROELECTRONICS AND PRINTED WIRING BOARDS ,TECHNOLOGY AND FABRICATION SUPPORT FOR
11647	THICK-FILM NETWORKS ,QUALIFICATION REQUIREMENTS FOR
11583	THICK-FILM PRINTING ,SCREEN - ESSENTIAL TOOL FOR
11607	THICK-FILM PROCESS ,DESPOSITION WEIGHT - POWERFUL CONTROL TOOL FOR
11604	THICK-FILM PROCESS ,PRACTICAL QUALITY CONTROL PLAN FOR
11586	THICK-FILM RESISTOR PASTES BY WEIGHT ,CALIBRATION OF
11580	THICK-FILM RESISTORS FOR MILITARY APPLICATIONS ,LASER-TRIMMING OF
11585	THICK-FILM RESISTORS UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN
11488	THICK-FILM RESISTORS WITH IMPROVED VOLTAGE STABILITY
11573	THICK-FILM RESISTORS ,IMPROVED SILVER-PALLADIUM TERMINATION METALLIZATION FOR
11623	THICK-FILM TECHNOLOGY ,METALLIC-OXIDE SWITCHES USING
11236	THICK-FILM WITH HIGH DIELECTRIC CONSTANT
11632	THICK-FILM ,TECHNOLOGY ASSESSMENT - SCREENPRINTING
11714	THICK-FILMS AND THIN-FILMS ,BASIC ADHESION MECHANISMS IN
11628	THIN SILICON-DIOXIDE ,CONTACT POTENTIAL MEASUREMENTS ON
11669	THING - CMOS CUSTOM DESIGN ,DOING YOUR OWN
11584	THIN-FILM AND THICK-FILM MICROCIRCUIT MANUFACTURE ,SEM PROCESS CONTROL OF

PAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11567	STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION
11730	STUDIES ,DESIGN AND USE OF LASER INTERFEROMETER FOR ULTRASONIC BONDING
11738	STUDIES ,FAMOS PROM RELIABILITY
11349	STUDIES ,PRACTICAL PROBLEMS IN APPLICATION OF ALUMINUM ELECTROMIGRATION FAILURE
11735	STUDIES ,PROGRESS REPORT ON NICHROME-LINK PROM RELIABILITY
11055	SYNTHESIS OF IC ELECTRICAL DIAGRAM FROM MASK DATA ,COMPUTER-AIDED
11457	SUBSTRATE TECHNOLOGY AND EPOXY COMPONENT ATTACH FOR HYBRID FABRICATION ,MULTILEVEL
11243	SUBSTRATES RELIABILITY CRITERIA - USER VIEW-POINT ,ALUMINA
11239	SUBSTRATES WITH BUMPS FOR FACE-DOWN BONDING OF HYBRID COMPONENTS ,PREPARATION OF
11582	SUBSTRATES ,FABRICATION ASSEMBLY AND TEST OF HYBRIDS ON EPOXY-FIBER GLASS
11727	SUBSTRATES ,GOLD ALUMINUM INTERMETALLICS ON THIN-FILM HYBRID MICROCIRCUIT
11619	SUBSTRATES ,INTEGRITY OF SOLDER JOINTS CONNECTING NICKEL LEADS TO THICK-FILM METALLIZATION ON CERAMIC
11277	SUBSTRATES ,VACUUM DEPOSITED SILICON DEVICES ON FUSED SILICA
11206	SUBSYSTEM DEVELOPMENT ,RADIATION HARDENED MOS INPUT/OUTPUT
11070	SUPERCONDUCTING TUNNEL DEVICES AS ALTERNATIVE TO SEMICONDUCTORS FOR FAST COMPUTER CIRCUITS
11302	SUPPORT FOR THICK-FILM MICROELECTRONICS AND PRINTED WIRING BOARDS ,TECHNOLOGY AND FABRICATION
11544	SURFACE ANALYSIS TECHNIQUES FOR DEPTH PROFILING OF MICROELECTRONIC MATERIAL ,PROBLEMS IN USING
11721	SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED MONOLITHIC SILICON IC'S ,STUDY OF
11654	SURFACE CLEANING BY ULTRAVIOLET RADIATION
11711	SURFACE CONTAMINATION ON THERMOCOMPRESSION BONDABILITY OF GOLD ,EFFECT OF
11298	SURFACE DESORPTION OF GASES FROM PHOTORESIST
11653	SURFACE OXIDE LAYERS BY X-RAY APPEARANCE POTENTIAL SPECTROSCOPY ,INVESTIGATION OF
11454	SURFACE PHOTOVOLTAGE DETECTION OF DEFECTS IN SILICON WAFERS ,SCANNED
11232	SURFACE POTENTIAL EQUILIBRATION METHOD OF SETTING CHARGE IN CCD'S
11541	SURFACE POTENTIALS ON IC'S AT HIGH-FREQUENCIES WITH SEM ,QUANTITATIVE DETERMINATION OF
11320	SURFACE REGIONS ON ELECTRICAL CONDUCTIVITY OF EXTRINSIC SEMICONDUCTOR FILMS ,EFFECT OF
11487	SURFACE STATES AT SILICON SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF LOW DENSITIES OF
11477	SURFACE ,FACTORS AFFECTING AVALANCHE INJECTION INTO INSULATING LAYERS FROM SEMICONDUCTOR
11425	SURFACES BY CONTACT ANGLE MEASUREMENTS ,CHARACTERIZATION OF THERMALLY GROWN SILICON-DIOXIDE
11424	SURFACES ,PLASMA CLEANING OF METAL
11343	SURVEY STUDY ,IC ELECTROMAGNETIC SUSCEPTIBILITY
11362	SURVIVABLE MOS COMPUTER DESIGN
11444	SUSCEPTIBILITY OF MICROWELDS IN HYBRID MICROCIRCUITS TO CORROSION DEGRADATION
11343	SUSCEPTIBILITY SURVEY STUDY - IC ELECTROMAGNETIC
11297	SUSCEPTIBILITY ,APPLICATION OF TIME DOMAIN METHODS TO IC
11513	SWITCH ,APPLICATIONS OF 10-OHM HIGH-SPEED ANALOG
11412	SWITCHES AND MULTIPLEXERS ,FOCUS ON IC ANALOG
11623	SWITCHES USING THICK-FILM TECHNOLOGY ,METALLIC-OXIDE
11426	SWITCHING IN SILICON-DIOXIDE ,ON NATURE OF CONDUCTION AND
11359	SYMPOSIUM ON SEMICONDUCTOR MEMORY TESTING - DIGEST OF TECHNICAL PAPERS ,1973
11568	SYMPOSIUM ,1974 INTERNATIONAL MICROELECTRONIC
11689	SYMPOSIUM ,PROCEEDINGS 1975 ANNUAL RELIABILITY AND MAINTAINABILITY
11635	SYMPOSIUM ,SEMICONDUCTOR MEASUREMENT TECHNOLOGY SPREADING RESISTANCE
11075	SYNCHRONIZING CIRCUIT FOR TV RECEIVERS USING IIL TECHNIQUES ,VERTICAL
11264	TAKES NEW DIRECTION WITH IIL ,BIPOLAR LSI
11388	TECHNOLOGICAL IMPLICATIONS IN PHOTOMASKING PROCESS
11709	TECHNOLOGICAL PROBLEMS IN GALLIUM-ARSENIDE ,INVESTIGATION OF
11182	TECHNOLOGIES ,RELIABILITY ASPECTS OF PROM
11248	TECHNOLOGY-400-12,SEMICONDUCTOR MEASUREMENT
11246	TECHNOLOGY-400-4 ,SEMICONDUCTOR MEASUREMENT
11247	TECHNOLOGY-400-8 ,SEMICONDUCTOR MEASUREMENT
11130	TELEVISION CAMERAS THROUGH HYBRID IC TECHNOLOGY ,MINIATURIZATION OF
11745	TEMPERATURE CYCLING OF PLASTIC AND CERAMIC IC'S WITH THERMAL-SHOCK PRECONDITIONING ,EXTENDED
11449	TEMPERATURE CYCLING ON ALUMINUM AND GOLD METAL SYSTEMS ,EFFECTS OF FAST
11486	TEMPERATURE INSTABILITIES IN MOS DEVICES ,NON-IONIC ROOM
11088	TENSILE STRENGTH OF THERMOCOMPRESSION BONDS ,TECHNIQUE FOR TESTING
11293	TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON ,LONG
11573	TERMINATION METALLIZATION FOR THICK-FILM RESISTORS ,IMPROVED SILVER-PALLADIUM
11731	TEST FOR BEAM-LEAD BOND INTEGRITY ,USE OF ACOUSTIC EMISSION AS 'ON-DESTRUCTIVE'
11563	TEST OF EBS-DIODE AT 200-300-WATT DISSIPATION ,LIFE
11582	TEST OF HYBRIDS ON EPOXY-FIBER GLASS SUBSTRATES ,FABRICATION ASSEMBLY AND
11442	TEST OF PARYLENE AS PROTECTIVE SYSTEM FOR MICROCIRCUITY
11476	TEST TECHNIQUES AS EFFECTIVE MICROCIRCUIT SCREENING METHODS ,EVALUATION OF HIGH-TEMPERATURE ACCELERATED LIFE
11056	TESTABLE 4K-RAM ,SIMPLIFIED PERIPHERAL CIRCUITS FOR MARGINALLY
11633	TESTERS - COMPONENTS IC'S PC-CARDS ASSEMBLIES
11593	TESTING AND NEED FOR STANDARDIZED FORMULATIONS ,CASE FOR BETTER EPOXY PERFORMANCE
11169	TESTING IC'S AT HIGH-TEMPERATURES
11367	TESTING OF COMBINATIONAL LOGIC CELLS IN LARGE-SCALE ARRAYS ,EFFICIENT

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11227	SOLID-STATE DEVICES ,CRUMP - ITS DEVELOPMENT AND USE IN SOLUTION OF PROBLEMS OF CONDUCTION HEAT FLOW IN
11638	SOLID-STATE LAMPS ,VAPOR DISPOSITION OF GALLIUM-PHOSPHIDE HIGH-EFFICIENCY YELLOW
11204	SOLID-STATE TRANSCEIVER ,INTEGRATED
11227	SOLUTION OF PROBLEMS OF CONDUCTION HEAT FLOW IN SOLID-STATE DEVICES ,CRUMP - ITS DEVELOPMENT AND USE IN
11400	SOME PITFALLS IN FAST RAMP C-V MEASUREMENTS
11327	SOME PRATICAL REMARKS ON DESIGN OF EXPERIMENTAL SYSTEMS FOR EXPITAXIAL GROWTH OF SI GE AND SI-GE
11364	SOS AND SPINEL ,COMPARSION OF SEMICONDUCTING PROPERTIES OF THIN-FILMS OF
11394	SOS CIRCUITRY ,RADIATION RESISTANT CMOS
11355	SOS IC TECHNOLOGY FORECAST
11439	SOS ISLAND EDGE PROFILES FOLLOWING OXIDATION
11251	SOS MOS MODELING FOR CIRCUIT DESIGN
11496	SOS PROCESSES FOR FABRICATION OF RADIATION HARDENED MIS DEVICES AND IC'S ,INVESTIGATION OF
11723	SOS RELIABILITY STUDY ,CMOS
11390	SOS TECHNOLOGY ADVANCES AND APPLICATIONS ,RECENT
11306	SOS TECHNOLOGY ,EVALUATION OF
11321	SOS ,ELASTORESISTANCE OF N-TYPE
11278	SOS ,HALL EFFECT IN
11710	SOS ,HIGH-SPEED CMOS
11561	SOURCES FOR FIBER OPTICAL COMMUNICATIONS ,RELIABILITY SEMICONDUCTOR LIGHT
11354	SOURCES ,PLANER DIFFUSION
11692	SPACE AGE SPIN-OFF TO ACHIEVE RELIABILITY AND LONG LIFE ,MICROCIRCUIT PACEMAKER
11157	SPACE STATION ,DESIGN PROCESSING AND TESTING OF LSI ARRAYS FOR
11374	SPACECRAFT ELECTRONIC SYSTEMS ,MULTILAYER INTERCONNECTION TECHNIQUE FOR IC AND THEIR APPLICATION TO
11376	SPACEPROGRAM ,HYBRID MICROCIRCUIT TECHNOLOGY IN BRITISH NATIONAL
11240	SPECIFICATION ,GOLD PLATING - EFFECT OF DESIGN
11414	SPECS ,BEWARE THOSE FET OP-AMP
11223	SPECS ,FACTS AND FALLACIES OF RADIATION HARD DEVICE
11653	SPECTROSCOPY ,INVESTIGATION OF SURFACE OXIDE LAYERS BY X-RAY APPEARANCE POTENTIAL
11497	SPEED CMOS/SOS CIRCUITS ,LOW-POWER HIGH
11364	SPINEL ,COMPARSION OF SEMICONDUCTING PROPERTIES OF THIN-FILMS OF SOS AND
11692	SPIN-OFF TO ACHIEVE RELIABILITY AND LONG LIFE ,MICROCIRCUIT PACEMAKER SPACE AGE
11608	SPOT IN-LINE QUALITY CONTROL SYSTEM FOR HYBRID MICROELECTRONIC ASSEMBLIES
11635	SPREADING RESISTANCE SYMPOSIUM ,SEMICONDUCTOR MEASUREMENT TECHNOLOGY
11082	SPUTTERING TECHNOLOGY ,NEW GEOMETRY IN
11080	SPUTTERING ,HIGH-RESOLUTION FABRICATION BY ION-BEAM
11656	SPUTTER-DEPOSITED GLASS FILMS ,PHYSICAL PROPERTIES OF THICK
11488	STABILITY ,THICK-FILM RESISTORS WITH IMPROVED VOLTAGE
11695	STANDARDIZATION ACQUISITION AND TECHNOLOGY ,MILITARY IC
11210	STANDARDIZATION ,COMPONENT TECHNOLOGY AND
11593	STANDARDIZED FORMULATIONS ,CASE FOR BETTER EPOXY PERFORMANCE TESTING AND NEED FOR
11665	STANDARD-PARTS LINE COMES OF AGE ,CMOS
11262	STATE TECHNOLOGY ,HIGHLIGHTS - SOLID
11487	STATES AT SILICON SILICON-DIOXIDE INTERFACE ,MEASUREMENT OF LOW DENSITIES OF SURFACE
11079	STATIC RAM WITH NORMALLY-OFF-TYPE SCHOTTKY BARRIER FET'S
11157	STATION ,DESIGN PROCESSING AND TESTING OF LSI ARRAYS FOR SPACE
11145	STATUS AND TRENDS IN US-GOVERNMENT DATA STORAGE APPLICATIONS ,BUBBLE MEMORY
11089	STATUS OF ACCELERATED TESTING OF IC'S ,PRESENT-DAY
11149	STICKY QUESTION ,EPOXY VS EUTECTIC BONDING -
11744	STIMULATED DISCHARGE EFFECTS IN POLYMER ENCAPSULANTS ,THERMALLY
11680	STIMULATED MEASUREMENTS - CHARACTERIZATION OF DEFECTS IN SILICON P-N JUNCTIONS ,THERMALLY
11145	STORAGE APPLICATIONS ,BUBBLE MEMORY STATUS AND TRENDS IN US-GOVERNMENT DATA
11652	STORAGE ARRAYS IN ESFI MOS TECHNOLOGY ,FULLY DECODED MNOS
11254	STORAGE BEHAVIOR IN METAL ALUMINA SILICON-DIOXIDE SILICON FET ,STUDY OF CHARGE
11736	STORAGE NON-VOLATILE MEMORY CELLS ,DUAL DIELECTRIC CHARGE
11365	STORAGE ,NON-VOLATILE CCD MEMORY WITH MNOS
11199	STRAPDOWN INERTIAL GUIDANCE USING LSI
11591	STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD ,CHANGES IN
11698	STRENGTH OF GOLD-PLATED COPPER LEADS ON THIN-FILM CIRCUITS UNDER ACCELERATED-AGING
11088	STRENGTH OF THERMOCOMPRESSION BONDS ,TECHNIQUE FOR TESTING TENSILE
11585	STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS UNDER HIGH-VOLTAGE
11292	STRESS ,ELECTRICAL PROPERTIES OF METAL SILICON-DIOXIDE SILICON STRUCTURES UNDER MECHANICAL
11465	STRESSING ,DETERMINATION OF USEFUL LIFE OF 2-LAYER METALLIZATION SYSTEMS VIA ACCELERATED
11378	STRESS-CORROSION CRACKING OF KOVAR PACKAGE LEADS ,METALLURGICAL ANALYSIS OF
11713	STRIPES ,ELECTROMIGRATION FAILURE IN NICHROME THIN-FILM
11542	STROBOSCOPIC TECHNIQUES ,INTERNAL WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC RAM USING SEM
11268	STRUCTURE DEPENDENCE OF FREE CHARGE-TRANSFER IN CCD'S
11547	STRUCTURE ,5000-CHANNEL POWER FET WITH NEW DIFUSSED GATE
11554	STRUCTURE ,ELECTRICALLY REPROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY WITH METAL NITRIDE MOLYBDENUM OXIDE SILICON
11546	STRUCTURE ,HIGH-POWER MOS FET WITH VERTICAL DRAIN ELECTRODE AND MESHED GATE
11702	STRUCTURES BY NUCLEAR AND ELECTRICAL TECHNIQUES ,ANALYSIS OF SEMICONDUCTOR
11292	STRUCTURES UNDER MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF METAL SILICON-DIOXIDE SILICON

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11698	THIN-FILM CIRCUITS UNDER ACCELERATED-AGING,STRENGTH OF GOLD-PLATED COPPER LEADS ON
11448	THIN-FILM CONDUCTORS ,ELECTROMIGRATION FAILURE IN GOLD
11591	THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM WIRE BONDS TO THICK-FILM AND
11727	THIN-FILM HYBRID MICROCIRCUIT SUBSTRATES ,GOLD ALUMINUM INTERMETALLICS ON
11726	THIN-FILM METALIZATION ,BERYLLIUM - HIGH-RELIABILITY
11098	THIN-FILM MULTILAYERING TECHNIQUE FOR HYBRID MICROCIRCUITS
11241	THIN-FILM NETWORKS ,DETECTION AND CORRECTION OF MATERIALS AND PROCESSES PROBLEMS IN
11569	THIN-FILM PASSIVATION ,TITANIUM NITROXIDE BURIED-LAYER
11579	THIN-FILM RESISTORS ,ON LASER-TRIMMING OF THICK-FILM AND
11416	THIN-FILM SILICON PROCESS FOR RADIATION HARDENED MIS IC'S ,INVESTIGATION OF
11713	THIN-FILM STRIPES ,ELECTROMIGRATION FAILURE IN NICHROME
11364	THIN-FILMS OF SOS AND SPINEL ,COMPARSION OF SEMICONDUCTING PROPERTIES OF
11640	THIN-FILMS ON SEMICONDUCTOR DEVICES ,REVIEW OF LIMITATIONS OF ALUMINUM
11103	THIN-FILMS UNDER CONSTANT AND REVERSED DC POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM
11714	THIN-FILMS ,BASIC ADHESION MECHANISMS IN THICK-FILMS AND
11734	THIN-FILMS ,FUSING MECHANISMS OF NICHROME
11484	THIN-FILMS ,ON DIRECTION OF ELECTROMIGRATION IN GOLD
11414	THOSE FET OP-AMP SPECS ,BEWARE
11663	THRUST IN DIGITAL LOGIC ,MOS - RCA PIONEERED TECHNOLOGY CMOS - RCA'S
11556	THYRISTOR - NEW COMPONENT ,FIELD CONTROLLED
11297	TIME DOMAIN METHODS TO IC SUSCEPTIBILITY ,APPLICATION OF
11522	TIME OF OP-AMPS ,RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND SETTLING
11069	TIME SHARED RECURSIVE FILTERS ,DUAL DIFFERENTIAL ANALOG CCD FOR
11668	TIMEKEEPING REVOLUTION THROUGH CMOS TECHNOLOGY
11618	TIME-DEPENDENT RELATIONSHIPS IN SOLAR INTERCONNECTIONS
11672	TIMES THROUGH COMPUTER-AIDED DESIGN ,KEEPING UP WITH
11569	TITANIUM NITROXIDE BURIED-LAYER THIN-FILM PASSIVATION
11471	TOGETHER ,L5 PHYSICAL DESIGN PUTS IT ALL
11052	TOLERANT A/D-CONVERTER ,HIGH-PRECISION COMPONENT
11133	TOLERANT GATED VIDEO AMPLIFIER ,RADIATION
11583	TOOL FOR THICK-FILM PRINTING ,SCREEN - ESSENTIAL
11607	TOOL FOR THICK-FILM PROCESS ,DESPOSITION WEIGHT - POWERFUL CONTROL
11724	TOOL IN ANALYSIS OF LSI SILICON CHIPS ,MICROSURGERY AS
11622	TOTAL INFRARED INTERNAL REFLECTION FOR CHARACTERIZATION OF ELECTRONIC FILMS ,ATTENUATED
11699	TOTAL-DOSE RADIATION HARDENED CMOS IC'S
11204	TRANSCEIVER ,INTEGRATED SOLID-STATE
11492	TRANSFER USING IMPULSE AND FREQUENCY RESPONSES ,MEASUREMENT OF CHARGE RESIDUAL FOR CCD
11543	TRANSFORMATION TO MODEL YIELD OF IC'S AS FUNCTION OF ACTIVE CIRCUIT AREA ,USE OF POWER
11651	TRANSISTOR CHARACTERISTICS ,DEPENDENCE OF SILICON-NITRIDE FILM THICKNESS ON BIPOLAR
11073	TRANSISTOR LOGIC ,SCHOTTKY
11275	TRANSISTOR MONOLITHIC INTEGRATION PROCESS ,CMOS AND COMPLEMENTARY ISOLATED BIPOLAR
11382	TRANSISTOR PRODUCTION ,PROCESS MONITORING IN
11567	TRANSISTORS FABRICATED WITH COMBINED OXIDE AND DIFFUSED ISOLATION STRUCTURES ,CHARACTERIZATION AND MODELING OF BIPOLAR
11397	TRANSISTORS FOR LOW-POWER IC'S ,BASE DIFFUSION ISOLATED
11312	TRANSISTORS ,DOUBLE EPITAXIAL ISOLATION METHOD FOR FABRICATION OF IC
11282	TRANSISTORS ,DRAIN VOLTAGE LIMITATIONS OF MOS
11272	TRANSISTORS ,ELECTRICAL CHARACTERISTICS OF BORON-IMPLANTED N-CHANNEL MOS
11523	TRANSISTORS ,HIGH SLEW RATE MONOLITHIC OP-AMP USING COMPATIBLE COMPLEMENTARY PNP
11548	TRANSISTORS ,HIGHLY RELIABLE HIGH-VOLTAGE
11064	TRANSISTORS ,HIGH-SPEED LOGIC LSI USING DIFFUSION SELF-ALIGNED ENHANCEMENT DEPLETION MOS
11470	TRANSISTORS ,REDUCED GAIN OF ION-IMPLANTED
11049	TRANSPARENT METAL OXIDE ELECTRODE CID IMAGER ARRAY
11195	TRANSPORT AND POLARIZATION EFFECTS IN DIELECTRICS OF MSI AND LSI DEVICES ,CHARGE
11300	TRANSPORT PROPERTIES OF CONDUCTION ELECTRONS IN N-TYPE INVERSION LAYERS IN <100>-SURFACES OF SILICON
11293	TRAPPING IMPURITIES IN SILICON ,LONG TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT
11641	TRAPPING IN CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING TREATMENTS ON CHARGE
11438	TRAPS ,TUNNEL INJECTION INTO GATE OXIDE
11641	TREATMENTS ON CHARGE TRAPPING IN CVD-ALUMINA FILMS ON SILICON ,EFFECTS OF POSTDEPOSITION ANNEALING
11296	TREES - PROGRAM ,COMPUTER GENERATED TROUBLESHOOTING
11382	TRENDS IN MICROWAVE POWER-TRANSISTORS
11145	TRENDS IN US-GOVERNMENT DATA STORAGE APPLICATIONS ,BUBBLE MEMORY STATUS AND
11613	TRIMMING OF FUNCTIONAL HYBRID MICROCIRCUITS ,ACTIVE LASER-TRIMMER FOR PRODUCTION
11614	TRIMMING PERFORMANCE FROM LASER SYSTEM ,METHOD OF OBTAINING OPTIMUM
11296	TROUBLESHOOTING TREES - PROGRAM ,COMPUTER GENERATED
11366	TTL COMPATIBLE MOS LOGIC ,VMOS - HIGH-SPEED
11514	TTL RAM TESTING ,BIPOLAR ECL AND
11104	TTL ,LOW-POWER SCHOTTKY
11401	TUNGSTEN METALIZATION FOR LSI APPLICATIONS
11070	TUNNEL DEVICES AS ALTERNATIVE TO SEMICONDUCTORS FOR FAST COMPUTER CIRCUITS ,SUPERCONDUCTING
11438	TUNNEL INJECTION INTO GATE OXIDE TRAPS
11456	TUTORIAL SESSIONS ON HYBRID TECHNOLOGY INTRODUCTION

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#

11075 TV RECEIVERS USING IIL TECHNIQUES ,VERTICAL SYNCHRONIZING CIRCUIT FOR
11135 UHF HYBRID INTEGRATED 45-WATT 2-STAGE AMPLIFIER WITH OCTAVE BANDWIDTH
11387 UHF POWER-TRANSISTORS,METALIZATION SYSTEM FOR MICROWAVE AND
11047 ULTRA HIGH-SPEED CLOCK-PULSELESS SCANNER FOR MOS IMAGE SENSORS
11576 ULTRA LOW-OHM CHIP RESISTORS
11730 ULTRASONIC BONDING STUDIES ,DESIGN AND USE OF LASER INTERFEROMETER FOR
11479 ULTRASONIC PROBE ,ELECTRICAL CONTACT THROUGH SILICON-DIOXIDE OVERLAY BY
11588 ULTRASONIC WIRE BONDING ON THICK-FILM CONDUCTORS ,RELIABILITY CONSIDERATION FOR
11590 ULTRASONIC WIRE BONDING ,HIGH RELIABILITY
11654 ULTRAVIOLET RADIATION ,SURFACE CLEANING BY
11698 UNDER ACCELERATED-AGING,STRENGTH OF GOLD-PLATED COPPER LEADS ON THIN-FILM CIRCUITS
11103 UNDER CONSTANT AND REVERSED DC POWERING ,ELECTROMIGRATION FAILURE IN ALUMINUM THIN-FILMS
11440 UNDER EXTERNAL PRESSURE - FORMULAS FOR SCREENING AND DESIGN ,RECTANGULAR FLAT-PACK LIDS
11585 UNDER HIGH-VOLTAGE STRESS AT RESTRICT CONDITION OF NO CURRENT-CARRYING ,RESISTANCE SENSITIVITY FOUND IN THICK-FILM RESISTORS
11292 UNDER MECHANICAL STRESS ,ELECTRICAL PROPERTIES OF METAL SILICON-DIOXIDE SILICON STRUCTURES
11517 UNDERSTANDING AND USING UNIQUE CMOS OP-AMP
11679 UNDOPED POLYSILICON INTERELECTRODE ISOLATION ,EFFECTS OF RADIATION ON BURRIED-CHANNEL CCD'S WITH DOPED POLYSILICON GATES AND
11265 UNDOPED POLYSILICON ,ELECTRONIC PROPERTIES OF
11243 USER VIEW-POINT ,ALUMINA SUBSTRATES RELIABILITY CRITERIA -
11145 US-GOVERNMENT DATA STORAGE APPLICATIONS ,BUBBLE MEMORY STATUS AND TRENDS IN
11739 UTILIZED AS PROM ELEMENTS ,ELECTRICALLY SHORTED SEMICONDUCTOR JUNCTIONS
11277 VACUUM DEPOSITED SILICON DEVICES ON FUSED SILICA SUBSTRATES
11638 VAPOR DISPOSITION OF GALLIUM-PHOSPHIDE HIGH-EFFICIENCY YELLOW SOLID-STATE LAMPS
11455 VARIATIONS ON NICHROME-LINK PROMS ,EFFECTS OF PROGRAMMING
11499 VERIFICATION OF CCD CONCEPT ,EXPERIMENTAL
11674 VERSATILE BUILDING BLOCK FOR MICRO-POWER DIGITAL AND ANALOG APPLICATIONS ,CMOS PLL -
11697 VERSUS ROUND WIRE RELIABILITY FOR HYBRID MICROCIRCUITS ,RIBBON WIRE
11546 VERTICAL DRAIN ELECTRODE AND MESHED GATE STRUCTURE ,HIGH-POWER MOS FET WITH
11075 VERTICAL SYNCHRONIZING CIRCUIT FOR TV RECEIVERS USING IIL TECHNIQUES
11465 VIA ACCELERATED STRESSING ,DETERMINATION OF USEFUL LIFE OF 2-LAYER METALLIZATION SYSTEMS
11133 VIDEO AMPLIFIER ,RADIATION TOLERANT GATED
11066 VIDEO BANDWIDTH CCD DELAY LINE ,MULTIPLEXED
11203 VIDEO PROTOTYPE MACHINE ,FABRICATION OF
11243 VIEW-POINT ,ALUMINA SUBSTRATES RELIABILITY CRITERIA - USER
11572 VISCOSITY CONTROL IN MULTILAYER GLASSES NEW CONCEPT ,HIGH-TEMPERATURE
11228 VISUAL INSPECTION ,TECHNIQUES OF FINAL PRESEAL
11366 VMOS - HIGH-SPEED TTL COMPATIBLE MOS LOGIC
11274 VMOS - NEW MOS IC TECHNOLOGY
11732 VOIDS ,NON-DESTRUCTIVE RADIOGRAPHIC INSPECTION OF CERAMIC CHIP CAPACITORS FOR DELAMINATIONS AND
11549 VOLTAGE IN PLANE AND PLANAR P-N JUNCTIONS ,SIMPLE ETCH CONTOUR FOR NEAR IDEAL BREAKDOWN
11282 VOLTAGE LIMITATIONS OF MOS TRANSISTORS ,DRAIN
11565 VOLTAGE OF CMOS IC'S ,LIMITATIONS ON MAXIMUM OPERATING
11488 VOLTAGE STABILITY ,THICK-FILM RESISTORS WITH IMPROVED
11149 VS EUTECTIC BONDING - STICKY QUESTION ,EPOXY
11409 VULNERABILITY ANALYSIS OF D/A-CONVERTER ,COMPUTER-AIDED
11393 WAFER TESTING
11454 WAFERS ,SCANNED SURFACE PHOTOVOLTAGE DETECTION OF DEFECTS IN SILICON
11602 WALLED MICROELECTRONICS PACKAGES ,DESIGN OF FLEXIBILITY OF GLASS
11611 WATCH PROTOTYPE ,THICK-FILM HYBRID ELECTRONIC
11489 WATER ABSORPTION IN CVD BOROSILICATE GLASS-FILMS
11542 WAVEFORM MEASUREMENTS OF MOS 3-TRANSISTOR DYNAMIC RAM USING SEM STROBOSCOPIC TECHNIQUES ,INTERNAL
11368 WAVEFORMS ON PERFORMANCE OF CCD'S ,INFLUENCE OF CLOCK
11607 WEIGHT - POWERFUL CONTROL TOOL FOR THICK-FILM PROCESS ,DESPOSITION
11586 WEIGHT ,CALIBRATION OF THICK-FILM RESISTOR PASTES BY
11219 WHAT ARE FACTS ,BEAM-LEADS -
11453 WIDTH DEPENDENCE OF ELECTROMIGRATION LIFE IN ALUMINUM-COPPER AL-CU-SI AND SILVER CONDUCTORS
11162 WIRE BOND RELIABILITY REPORT ,RE-APPRAISAL OF RAC MICROCIRCUIT
11588 WIRE BONDING ON THICK-FILM CONDUCTORS ,RELIABILITY CONSIDERATION FOR ULTRASONIC
11590 WIRE BONDING ,HIGH RELIABILITY ULTRASONIC
11728 WIRE BONDS TO GOLD METALLIZATION ,METALLURGICAL ASPECTS OF ALUMINUM
11591 WIRE BONDS TO THICK-FILM AND THIN-FILM GOLD ,CHANGES IN STRENGTH AND RESISTANCE AFTER BURN-IN OF ALUMINUM
11697 WIRE RELIABILITY FOR HYBRID MICROCIRCUITS ,RIBBON WIRE VERSUS ROUND
11697 WIRE VERSUS ROUND WIRE RELIABILITY FOR HYBRID MICROCIRCUITS ,RIBBON
11443 WIRES AND SEALING GLASSES WITH EXTENDED THERMAL CYCLING ,DEGRADATION OF BONDING
11729 WIRES BONDED TO GOLD METALLIZATION IN MICROSUBSTRATES ,INVESTIGATION INTO FAILURES OF ALUMINUM
11140 WIRES IN HIGH-ACCELERATION HYBRID APPLICATIONS ,1-MIL GOLD
11302 WIRING BOARDS ,TECHNOLOGY AND FABRICATION SUPPORT FOR THICK-FILM MICROELECTRONICS AND PRINTED
11653 X-RAY APPEARANCE POTENTIAL SPECTROSCOPY ,INVESTIGATION OF SURFACE OXIDE LAYERS BY
11437 X-RAY PHOTOELECTRON SPECTROSCOPY ,SODIUM-IONS AT DEFECT SITES AT SILICON-DIOXIDE SILICON INTERFACES AS DETERMINED BY

RAC LIBRARY DOCUMENT TITLE -- KEY WORD IN CONTEXT REPORT (1976 ACCESSIONS ONLY)

DOC-ACC#	
11467	X-RAY RADIATION-EFFECTS ON SEMICONDUCTOR DEVICES
11638	YELLOW SOLID-STATE LAMPS ,VAPOR DISPOSITION OF GALLIUM-PHOSPHIDE HIGH-EFFICIENCY
11543	YIELD OF IC'S AS FUNCTION OF ACTIVE CIRCUIT AREA ,USE OF POWER TRANSFORMATION TO MODEL
11587	YIELDS AS FUNCTION OF PHYSICAL DESIGN PARAMETERS ,FINE-LINE SCREEN PRINTING
11603	YIELDS IN HYBRID PACKAGE HERMETIC SEALING - PROCESS CONTROL IS ANSWER ,HOW TO ACHIEVE AND MAINTAIN HIGH
11083	YIELDS NEW GENERATION OF MICROPROCESSORS ,N-CHANNEL MOS TECHNOLOGY
11669	YOUR OWN THING - CMOS CUSTOM DESIGN ,DOING

☆U.S. GOVERNMENT PRINTING OFFICE: 1976-714-035/68